MODEL 561
SCALAR NETWORK ANALYZER

MAINTENANCE MANUAL

WILTRON

490 JARVIS DRIVE • MORGAN HILL, CA 95037-2809
TEL. (408) 778-2000 • TELEX 285227 WILTRON MH • FAX 408-778-0239

P/N: 10410-00020
REVISION: A
PRINTED: APRIL 1989

The 561 is equally effective in waveguide reflectometer setups, where ratio measurements may be preferred. The 560-10BX-1 Adapter Cables provide the interface between the instrument and waveguide detectors.

1-6.3 Cursors, Markers, and Limit Lines

The 561 has extensive cursor functions available on a scalar network analyzer. These cursor functions are in addition to the eight markers available when the WILTRON 6600B Sweep Generator is used as the system signal source. Through a dedicated GPIB link, the 561 communicates with the signal source and displays an identifier for each marker.

To speed the interpretation of data, complex limit lines can be entered through the front panel or the GPIB interface. Limit lines can have up to ten segments which slope or step with frequency.

1-6.4 Averaging and Smoothing

When characteristics of the test device vary rapidly with frequency at very low signal levels, the trace can be smoothed by averaging and/or smoothing. The smoothing control has three selections: Off, Min, and Max. To maintain the accuracy of the measurement data, smoothing is performed by reducing bandwidth, rather than by averaging adjacent data points in order to preserve measurement detail.

When averaging is selected, 4 to 256 successive traces can be averaged to smooth the trace display. As various combinations of smoothing and averaging are selected, the trace update time is automatically adjusted.

1-6.5 Measurement Accuracy

The return-loss accuracy of the 561 is largely attributable to the high directivity of the WILTRON SWR Autotesters. For example, the 560-97A50-1 with its GPC-7 test port connector has a directivity of better than 40 dB from 10 MHz to 18 GHz. On the 560-98K50, the directivity exceeds 35 dB up to 18 GHz, 32 dB up to 26.5 GHz, and 30 dB up to 40 GHz. The same unit has a test port match of better than 23 dB up to 26.5 GHz and 15 dB up to 40 GHz. To avoid the use of error-producing adapters, SWR Autotesters are available with either male or female test ports in Type N, WSMA, or K Connectors. All have high directivity. When the GPC-7 test port is selected, the lowest reflection adapters obtainable are offered in Type N and WSMA, which is optimized for testing SMA devices.

The accuracy of a transmission loss, gain, or power measurement is affected by reflections from the test port, the device under test, and the detector. These errors are minimized by the very low reflections from the WILTRON SWR Autotesters and detectors.

Zero-biased Schottky diodes are used in all detectors to minimize drift and circuit complexity. Diode modules are field-replaceable. This eliminates the expense and inconvenience of returning the detectors to a service center for repair.

The accuracy of the 561 is high also because modulation of the input signal is not required. The need for modulation is avoided by using self-balancing amplifiers, which are stable at low signal levels. As a result, errors from modulation asymmetry and modulation-sensitive test devices are nonexistent. Without the insertion loss of a modulator, measurements can be made at higher input levels. This increases the measurement dynamic range.

1-6.6 Recommended Signal Sources

There are many advantages in selecting the WILTRON 6600B Sweep Generator as the 561 signal source. One advantage is the power sweep. In this mode, the output power is swept over a 15 dB range, enhancing gain compression measurements. In the alternate sweep mode, the 561 can display frequency response over different frequency ranges and/or power levels.

Another advantage of using a WILTRON signal source is that the 6600B uses fundamental oscillators from 2 to 26.5 GHz, avoiding the serious errors introduced by the subharmonics of frequency multipliers.

1-6.7 Stored Test Setups

Set-up time is reduced substantially by storing up to nine front-panel setups, four of which include their own calibration data. A unique preview feature allows stored setup parameters to be reviewed before recalling or storing a new setup in the memory location. The stored data are backed by a battery with an estimated 10-year life.

1-6.8 GPIB Compatibility

An IEEE-488 General Purpose Interface Bus (GPIB) interface is standard, providing remote control of all front-panel functions except power on/off and CRT intensity. A high speed data transfer can be used to transfer measurement data to the host computer. This capability is especially useful in manufacturing environments where archiving of data is required.

1-7 OPTIONS

The following standard instrument option is available.

Option 1, Rack Mount. A kit is available containing mounting brackets and chassis track slides. Also, mounting ears and a chassis track slide with a 90° tilt are provided.

1-8 ADDITIONAL EQUIPMENT REQUIRED

Either of the following equipment, shown in Figure 1-4, is required for 561 operation.

1-8.1 SWR Autotester

The 560 Series SWR Autotesters integrate in one small package a broadband, high directivity bridge, a detector, a low reflection test port, a reference termination, and a connecting cable. The output of the SWR Autotester is a detected signal, varying in proportion to reflections from the test device connected to the test port. Optional extender cables can be used without degradation in performance.

1-8.2 Detectors

The 560 Series detectors are used for coaxial transmission loss or gain and power measurements and with coaxial adapters for waveguide reflectometer measurements. Zero-biased, field-replaceable Schottky diodes provide –60 dBm sensitivity. Optional extender cables can be used without degradation in performance.

1-9 AVAILABLE ACCESSORIES

The following accessories, shown in Figure 1-5, are available for the 561.

1-9.1 Extender Cables

Extender cables can be installed between the SWR Autotester or detectors and the 561, permitting measurements up to 200 feet. The available lengths are:

- 7.6m (25 ft.);
- 15.2m (50 ft.);
- 30.5m (100 ft.);
- 61m (200 ft.).

1-9.2 GPIB Cables

GPIB cables interconnect instruments on GPIB. The available lengths are:

- 1m (3.3 ft.);
- 2m (6.6 ft.);
- 4m (13.2 ft.);
- 0.5m (1.65 ft.).

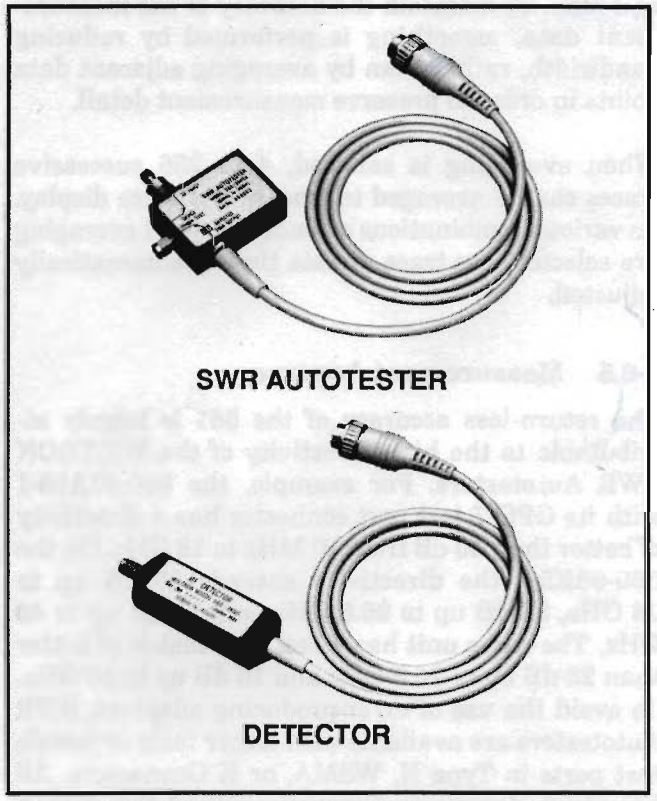

Figure 1-4. 560 Series SWR Autotester and Detector

1-9.3 Adapter Cables

Adapter cables with BNC and SMA female connectors allow the 561 to be used with waveguide or other detectors with the same type of output connectors. Cable length is 122 cm (4 ft.).

1-9.4 Open/Short Calibration References

An Open/Short is used to establish a 0 dB return loss reference during the normalization procedure. The available connectors are:

- GPC-7 Short Only;
- GPC-7;
- K Male;
- K Female;
- N Male;
- N Female;
- WSMA Male;
- WSMA Female.

1-9.5 Other Accessories

Other accessories for the 561 include:

- A transit case for the RF components;
- A transit case for the instrument itself;
- A 260 mm (10.25 in.) diagonal external monitor;
- An ink jet printer, including a 2225-1 Interface Cable, 1 ink cartridge, and 50 sheets of Ink Jet paper.

1-10 PERFORMANCE SPECIFICATIONS

Performance specifications for the 561 are listed in Section 1 of the Operating Manual and Section 2 of this manual.

1-11 RECOMMENDED TEST EQUIPMENT

Table 2-1 provides a list of recommended test equipment needed to check and service the 561 Network Analyzer.

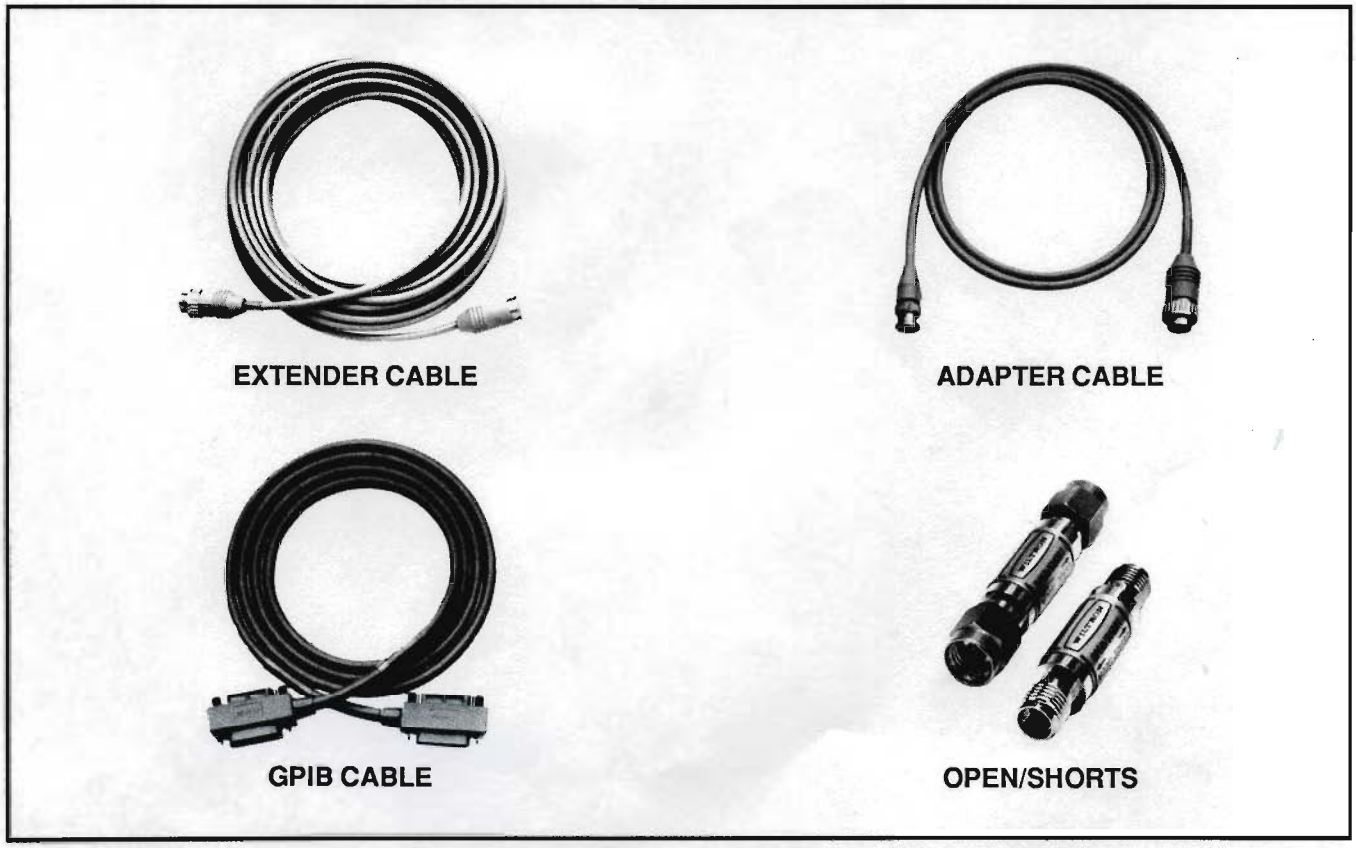

Figure 1-5. Available Accessories for the 561

CONTENTS

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

SECTION 1
GENERAL INFORMATION

CONTENTS

Figure1-1. 561 Scalar Network Analyzer

SECTION I
GENERAL INFORMATION

1-1 SCOPE OF THE MANUAL

This manual provides general information, performance verification, calibration, parts lists, and service information for the 561 Network Analyzer.

1-2 INTRODUCTION

Section I provides a general description of the equipment, its identification number, other related manuals, performance specifications, and options. A list of recommended test equipment is also given.

1-3 IDENTIFICATION NUMBER

All WILTRON instruments are assigned a unique six-digit ID number, such as K 701001. Each 561 has an ID number affixed to the outside of the rear panel. Please use this number when ordering parts or corresponding with WILTRON's Customer Service department.

1-4 RELATED MANUALS

This is one of a two manual set that consists of an Operating Manual (OM) and a Maintenance Manual (MM). The WILTRON part number for this manual is listed on the title page.

1-5 NETWORK ANALYSIS DESCRIPTION

Network analysis includes the characterization of microwave devices through the measurement of their transmission and impedance characteristics as a function of frequency. It includes the measurement of input match, output match, forward transmission, and reverse transmission. Each of these parameters is a complex quantity consisting of magnitude and phase.

A network analyzer system consists of three main elements: the signal source, the measurement components, and the network analyzer or signal processing element. There are two basic types of network analyzers: scalar and vector. Scalar network analyzers measure only the magnitude of the transmission or reflection signal. Vector network analyzers measure the magnitude and the phase of the transmission or reflection parameter. The 561 is a scalar network analyzer signal processor. An external signal source must be used with the 561.

1-6 561 SCALAR NETWORK ANALYZER DESCRIPTION

The Model 561, shown (Figure 1-1), is a scalar network analyzer that has a frequency range of 10 MHz to 40 GHz and a dynamic range of 71 dB. It is ideal for both production and R&D applications.

1-6.1 Measurement System Overview

With the addition of a sweep generator, the 561 becomes an automated transmission, return loss (SWR), and power measurement system. Operating over the 10 MHz to 40 GHz range from a single coaxial test port, the system provides fully annotated displays of test data and measurement parameters (Figure 1-2).

Under internal microprocessor control (no external controller required), the 561 normalizes and simultaneously displays any two inputs on channels A, B,R1, and R2. The same inputs can be displayed as ratios A/R1, A/R2, B/R1, or B/R2. The dynamic range for each channel is 71 dB (–55 dBm to +16 dBm). Typically, the noise floor is less than –62 dBm, providing a greater than 76 dB dynamic range in almost all applications.

Key 561 features include:

- Automatic measurements and hard copy output without a controller:
- Accurate coaxial measurements from 10 MHz to 40 GHz:
- Nine stored setups to eliminate set-up time:
- Cursors, markers, and limit lines to improve productivity:
- Complete, annotated, step-by-step normalization and measurement procedures:
- Four measurement channels:
- Low cost network analyzer.

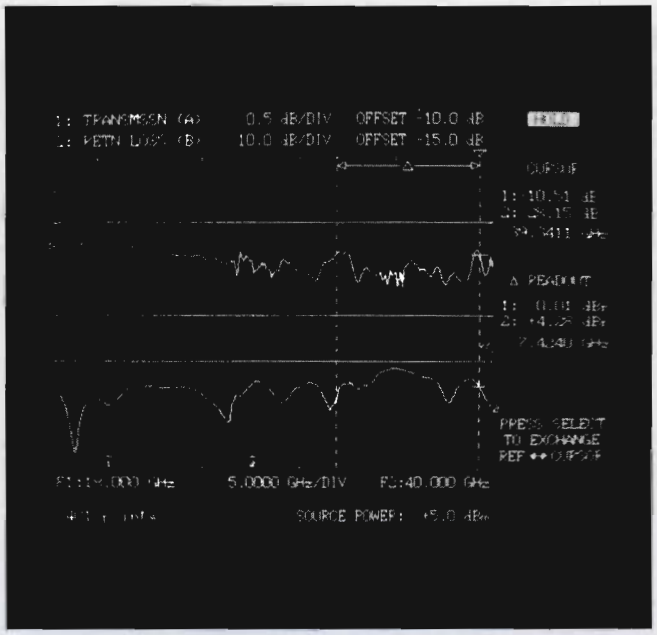

Figure 1-2. Typical 561 Annotated Display

1-6.2 Normalization and Measurement

In a typical 561 test setup, the test device is inserted between the SWR Autotester and the detector (Figure 1-3). Detected signals from the SWR Autotester vary in proportion to the reflections, while the detector output varies in proportion to transmission loss or gain. The detector can be used to measure power in dBm.

During normalization, procedural guidance is automatically provided for transmission and return loss measurements. For a return loss test, a 0 dB reference is established by connecting an open, then a short, to the SWR Autotester test port. The normalization data are taken independent of sensitivity settings at up to 2001 points, with 0.002 dB resolution, and stored in memory for correction of test data or for recall. Furthermore, an algoritrm interpolates between data points to hold interpolated test data accuracy usually within ±0.1 dB. Therefore, once the 561 has been normalized across a user-selected frequency range, measurements can be made over any portion of the range without renormalization. Set-up time is virtually eliminated by storing parameters for up to nine test setups.

During measurements, data are taken at 101, 201, or 401 points (user selected) with 0.002 dB vertical resolution on both channels. Typically, test data are updated every 100 ms, allowing "real time" adjustments of the test device. A permanent record of the test data – with or without the test, marker, or stored setup parameters – is made automatically on an HP 7440A, 7470A, or 7475A plotter or on most dot-matrix printers, including the Epson FX and the optional WILTRON 2225C Ink Jet Printer. Since the 561 requires only about 10 seconds for print formatting, a new test can be conducted while the previously taken data are being printed out.

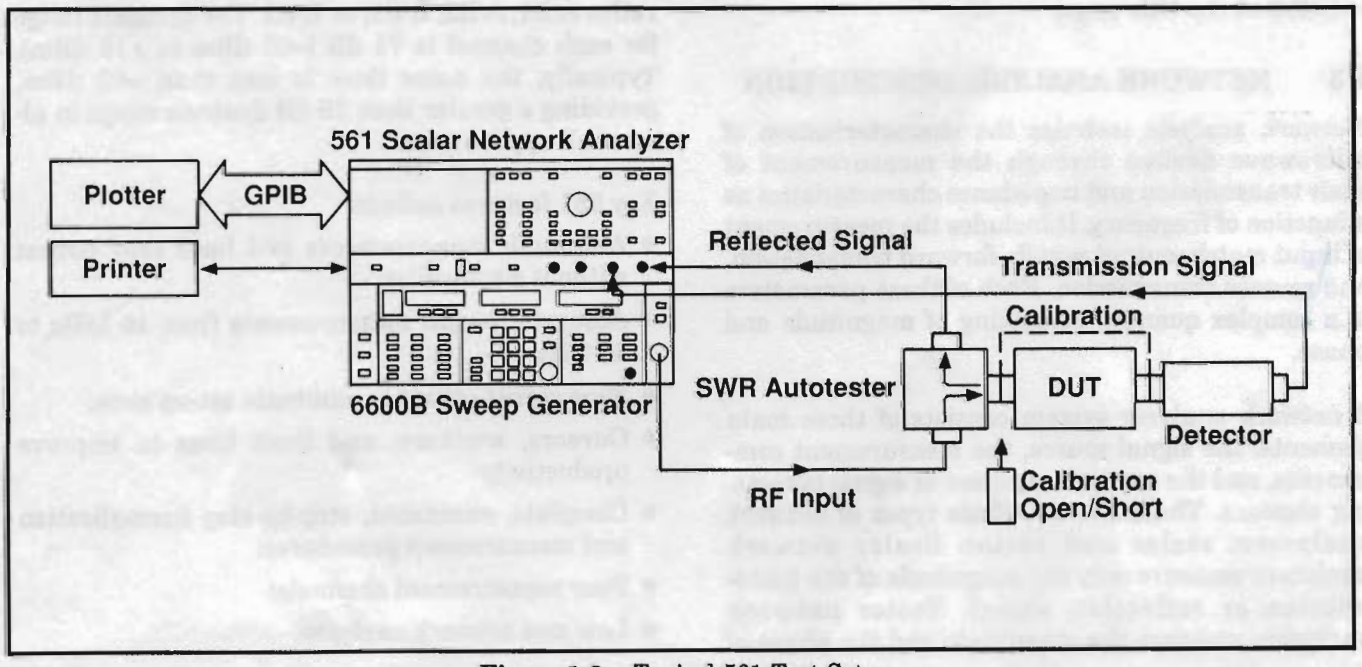

Figure 1-3. Typical 561 Test Setup

SECTION 2
PERFORMANCE VERIFICATION

CONTENTS

Table 2-1. Recommended Test Equipment

Instrument	Required Characteristics	Recommended Manufacturer	Test Method*
Sweep Generator	1. Provide compatible signals for 561 HORIZ IN and SEQ SYNC input and DWELL output 2. Have output power of +10 dBm at 50 MHz (RF method)*	WILTRON Model 6647B with Option 3	DC, RF
Connector Cable	To connect sweep generator signal for 561 compatiblity	WILTRON 806-7	DC, RF
GPIB Cable	To connect 561 to 6647B via dedicated bus	WILTRON 2100-1 or -5	RF
Voltage Standard	Range: –1.462 Vdc to –1.313 mVdc Accuracy: 0.002% of setting +10 μV	Fluke Model 335A	DC
Adapter Cable	Contains precise-resistor values that simulate Model 5607 Series RF detectors	WILTRON Model 560-10BX	DC
Adapter	BNC Female-to-Double Banana Plug	ITT Pomona Elect. Model 1269	DC
Step Attenuator	60 dB range	HP 355D	RF
Power Meter	50 MHz calibrated output	HP 436A	RF
Power Sensor	Power range covering 0, –5 dBm	HP 8481	RF
Adapters (50 Ohm Impedance)	Type N (male) to BNC (male) Type N (female) to BNC (male)	HP 1250-0176 HP 1250-0082	RF
561 Extender PCB	Used on the A4 PCB during the Sweep Ramp Amplifier Gain Adjustment (paragraph 3-4)	WILTRON 561-D-32561-1	N/A

* This section describes two methods of performance verification; the DC Method (paragraph 2-3.1) and the RF Method (paragraph 2-3.2).

SECTION 2
PERFORMANCE VERIFICATION

2-1 INTRODUCTION

This section provides two procedures for verifying signal channel accuracy; RF and DC. This is the only test necessary to ensure that the 561 provides proper performance. The two procedures provide alternative methods for checking signal channel accuracy.

2-2 RECOMMENDED TEST EQUIPMENT

Table 2-1 (facing page) provides a listing of recommended test equipment for both the DC and RF methods. If the recommended items are not available, equipment with equivalent characteristics may be substituted.

2-3 VERIFYING SIGNAL CHANNEL ACCURACY

This section provides two methods for verifying signal channel accuracy. The first and most accurate is the DC Voltage Method, which uses highly accurate voltages applied directly to the signal channel. When using this method, any measurement uncertainty is negligible when the recommended equipment is used. The second is the RF Method which has measurement uncertainties attributable to the source, attenuator, and detector.

2-3.1 DC Voltage Method

The DC Voltage Method uses highly accurate dc voltages to simulate input RF power without introducing source errors. A 560-10BX adapter cable must be used to connect the dc voltage to the input of the 561.

1. Set up the test equipment as shown in Figure 2-1.
2. With the 561 off, press the POWER key on the 6647B and allow the self test to finish.
3. Press the RESET key on the 6647B.
4. Press the POWER key on the 561 and allow the self test to finish.

NOTE

Unless otherwise specified, the 561 is the instrument referred to in the following steps.

5. Press the SYSTEM RESET key.
6. Using the MENU up/down keys, highlight RESET.
7. Press the SELECT key.
8. Press the Channel 2 DISPLAY ON/OFF key to turn off its corresponding LED.
9. Press the Channel 1 MENU key.
10. Using the MENU up/down keys, highlight POWER.

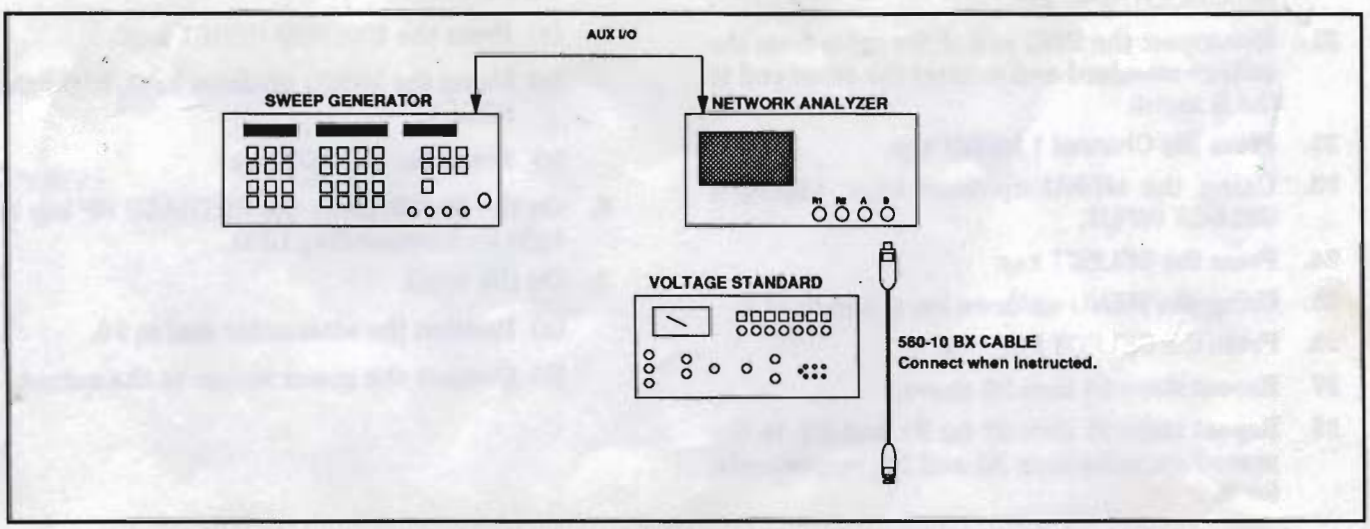

Figure 2-1. Test Equipment Setup for Signal Channel Accuracy Test, DC Voltage Method

11. Press the SELECT key.
12. Connect the 560-10BX cable to the A input. Leave the BNC end of the cable disconnected.
13. Press the CURSOR ON/OFF key to light the CURSOR LED.
14. Press the CALIBRATION key.
15. Using the MENU up/down keys, highlight LOW LVL TRIM.
16. Press the SELECT key twice. Wait until the NULLING message disappears and a cursor display appears.
17. Adjust the voltage standard to provide voltage 1 in Table 2-2.
18. Connect the BNC end of the cable to the voltage standard.
19. On the 561, verify that the CURSOR dBm value displayed in the menu area is within the tolerances listed in Table 2-2.

Table 2-2. DC Voltage Chart

Number	DC Voltage	CURSOR dBm Reading
1	–1.462V	+16 +0.25/–0.10 dBm
2	–0.6208V	+9 +0.12/–0.10 dBm
3	–1.313 mV	–26 ±0.34 dBm

20. Increment the voltage standard output to voltages 2 and 3, in turn, and verify that the displayed CURSOR dBm value is within the tolerances listed in Table 2-2. When using voltage 3, set SMOOTHING to MIN by pressing the SMOOTHING key.
21. Disconnect the BNC end of the cable from the voltage standard and connect the other end to the B input.
22. Press the Channel 1 MENU key.
23. Using the MENU up/down keys, highlight SELECT INPUT.
24. Press the SELECT key.
25. Using the MENU up/down keys, highlight B.
26. Press the SELECT key.
27. Repeat steps 14 thru 20 above.
28. Repeat steps 21 thru 27 for R1 and R2. In the procedure, substitute R1 and R2, respectively, for B.

2-3.2 RF Test Method

The RF method for verifying signal channel accuracy is inherently inaccurate. Tables 2-3 and 2-4 detail these uncertainties. These uncertainties are explained in paragraph 2-4. Tables 2-3 and 2-4 show errors that are inherint to the recommended test equipment setup, and not to the 561.

a. Power Meter/Power Sensor Calibration at 50 MHz

1. Position the CAL FACTOR control on the power meter to the necessary calibration power factor as specified on the power sensor chart.
2. Zero the power meter.
3. Connect the power sensor to the POWER REF connector. With the POWER REF ON, adjust the CAL ADJ potentiometer for 0.00 dBm on the power meter display.
4. Disconnect the power sensor from the POWER REF connector.

b. Sweep Generator/Step Attenuator Output Power Calibration

1. Set up the test equipment as shown in Figure 2-2.
2. With the 561 off, press the POWER key on the 6647B and allow the self test to finish.
3. Press the RESET key on the 6647B.
4. Press the POWER key on the 561 and allow the self test to finish.
5. On the 561:
   (a) Press the SYSTEM RESET key.
   (b) Using the MENU up/down keys, highlight RESET.
   (c) Press the SELECT key.
6. On the 6647B, press the RETRACE RF key to light its corrsponding LED..
7. On the 355D:
   (a) Position the attenuator dial to 10.
   (b) Connect the power sensor to the output.

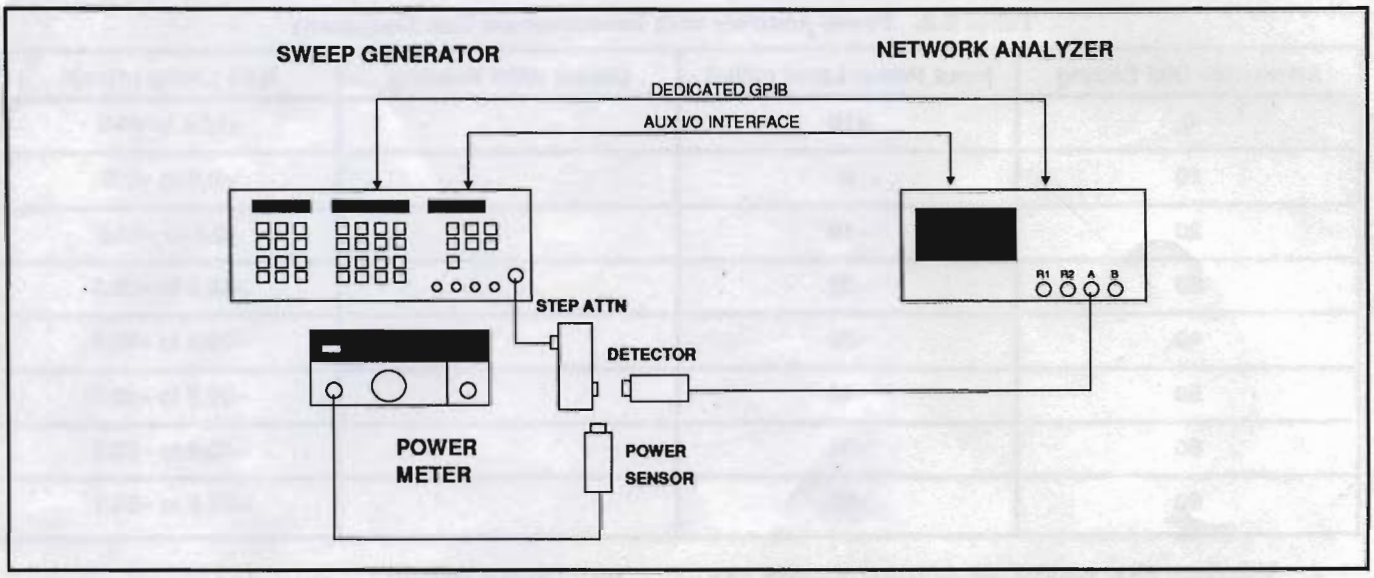

Figure 2-2. Test Equipment Setup for Signal Channel Accuracy Test, RF Method

8. On the 6647B:
   (a) Press ΔF CF and set the frequency to 50 MHz.
   (b) Set ΔF to 0 MHz
   (c) Press LEVEL and set the output power for +5 dBm (nominal) using the keypad.
   (d) Using the DECR-INCR control, adjust the output power to indicate –5 dBm on the power meter display.
   (e) Record the indicated output power level from the LEVEL display.
   (f) Set the level to +10 dBm (nominal) using the keypad.
   (g) Using the DECR-INCR control, adjust the output power to indicate 0.00 dBm on the power meter display.
   (h) Record the indicated output power level from the LEVEL display.

c. *Channel A Power Accuracy Test*

1. On the 355D:
   (a) Remove the power sensor.
   (b) Connect the detector.
   (c) Set the dial to 0.
2. On the 6647B, press the RETRACE RF key to turn off its corresponding LED.
3. On the 561:
   (a) Press the Channel 2 DISPLAY ON/OFF key to turn off the Channel 2 display.
   (b) Press the Channel 1 MENU key.
   (c) Using the MENU up/down keys, highlight POWER.
   (d) Press the SELECT key.
   (e) Press the CURSOR ON/OFF key to turn on the cursor display.

Table 2-3. Power Accuracy with Recommended Test Equipment

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	RSS Limits (dBm)*
0	+10		+10.6 to +9.5
10	0		+0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

4. Tabulate the results as follows: Record the CURSOR readout from the display into Table 2-3, on the line for the corresponding Attenuator Dial Setting.
5. On the 355B and 561, tabulate as in step 4, above, for settings of 10, 20, 30, and 40.

NOTE

Smoothing should be off for the above attenuator settings.

6. Position the 355D to 50.
7. On the 561:
   (a) Press the SMOOTHING key to light the MIN indicator.
   (b) Press the AVERAGING key.
   (c) Use the MENU up/down keys to highlight 4 SWEEPS and SELECT.
   (d) Tabulate the results as described in step 4, above.
8. Position the 355D to 60.
9. On the 561:
   (a) Press the SMOOTHING key to light the MAX indicator.
   (b) Press the AVERAGING key.
   (c) Press SELECT (this starts the averaging).
   (d) Tabulate as described in step 4, above. The readout corresponds to a –50 dBm input power level.
10. On the 6647B:
    (a) Press the LEVEL key, and using the keypad enter the level as recorded during the Sweep Generator/Step Attenuator Output Power Calibration in step b.8(e).
    (b) Averaging starts automatically when the 6647B changes level.
    (c) Tabulate as described in step 4, above. The readout corresponds to –55 dBm input power level.

d. Channel B Power Accuracy Test

1. On the 561:
   (a) Press the SMOOTHING key to OFF.
   (b) Press the AVERAGING key twice to turn averaging off.
   (c) Press the Channel 1 MENU key.
   (d) Using the MENU up/down keys, highlight SELECT INPUT.
   (e) Press the SELECT key.
   (f) Using the MENU up/down keys, highlight B.
   (g) Press the SELECT key.
   (h) Move the detector to the B input.
   (i) Press the CURSOR ON/OFF key to restore the cursor display in the menu area.

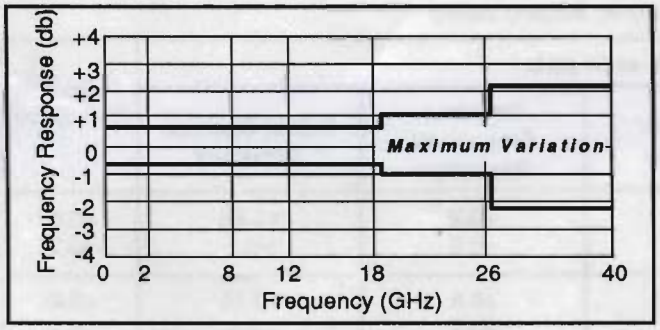

Figure 2-3. Detector Frequency Response

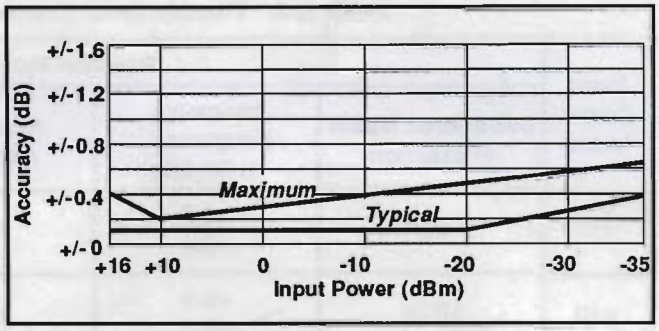

Figure 2-4. Channel Accuracy

2. On the 6647B:
   (a) Press the LEVEL key.
   (b) Using the keypad and appropriate terminator key, set the output power for the value recorded in step b.8(h).
3. On the 355D, position the attenuator dial to 0.
4. Repeat steps c.4 thru c.10, above.

e. Channels R1 and R2 Power Accuracy Tests
Repeat the procedure in paragraph 2-3.2d, steps 1 thru 4, for inputs R1 and R2. Subsititute R1 and R2, respectively, for B.

2-4 INHERENT UNCERTAINTIES IN RF TEST METHOD

The power measurement system using the recommended test quipment listed in Table 2-1 and shown in Figure 2-2 contains inherent measurement uncertainties. These uncertainties are explained in the following paragraphs.

a. Detector/Source Match Interaction Uncertainty
The impedance mismatch between the RF source and the RF detector contributes a possible uncertainty known as source match. For the 6647B and the 560-7 Series detectors, this uncertainty is as follows:

- At +10 dBm (355D Attenuator Dial at 0), the source match of the sweeper and the mismatch of the RF detector interact to produce an overall uncertainty of ±0.28 dB.
- At 0 dBm and below (355D Attenuator Dial between 10 and 60), the source match of the 355D and the RF detector interact to produce an uncertainty of ±0.14 dB.

b. Sweep Generator Harmonics
In the linear range of the RF detector (between +16 dBm and approximately –15 dBm) harmonics of the sweep generator fundamental frequency contribute to errors in the measurement.

c. Step Attenuator Accuracy
The HP355D step attenuator has a specified accuracy of ±0.3 dB from dc to approximately 50 MHz. This possible error in accuracy is present at all attenuator dial settings, including zero.

d. Detector Frequency Response
The frequency response of the Model 560-7 detector introduces a further possible error as shown in Figure 2-3.

e. Signal Channel Accuracy
The accuracy varies with input power as shown in Figure 2-4. Be advised that the values used in Table 2-4 are factory test values. They are much tighter than the published accuracy as shown in Figure 2-4.

Table 2-4. Possible Error Sources Effect on Measurement

Input Power (dBm)	Possible Error (dB) at 50 MHz					RSS Error
	Det/Source Match Interaction	Harmonic Frequency at 30 dBc	Attenuator Accuracy	Detector Frequency Response	Signal Channel Accuracy	
+16	±0.31	+0.6 –0.4	±0.3	+0.3 –0.2	+0.25 –0.1	+0.8 –0.7
+10	±0.28	+0.3 –0.2	±0.3	+0.3 –0.2	+0.15 –0.1	+0.6 –0.5
0	±0.14	+0.3 –0.2	±0.3	+0.3 –0.2	±0.2	+0.6 –0.5
–10	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.25	+0.6 –0.5
–20	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.3	+0.6 –0.5
–30	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.4	+0.7 –0.6
–40	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.5	±0.7
–50	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±0.8	+1.0 –0.9
–55	±0.14	+0.15 –0.1	±0.3	+0.3 –0.2	±1.0	±1.1

2-5 PERFORMANCE TEST RECORD

A blank copy of a sample performance test record is provided below. This test record provides the means for maintaining an accurate and complete record of instrument performance. We recommend that you copy these pages and record on them the results from your initial testing of the 561. These initial readings can later be used as benchmark values for future tests of the same serial-numbered instrument.

2-5.1 DC Test Method

The tables on page 2-9 provide a place for recording the voltages actually measured for Inputs A, B, R1 and R2 .

2-5.2 RF Test Method

The tables on pages 2-10 and 2-11 provide a place for recording the voltages actually measured for Inputs A, B, R1 and R2 .

Input A, Channel 1

Number	DC Voltage	CURSOR dBm Reading	CURSOR Reading (dBm)
1	1.462V	+16,+0.25/–0.10	
2	–0.6208V	+9 +0.12/–0.10	
3	–1.313 mV	–26 ±0.34	

Input B, Channel 1

Number	DC Voltage	CURSOR dBm Reading	CURSOR Reading (dBm)
1	1.462V	+16 +0.25/–0.10	
2	–0.6208V	+9 +0.12/–0.10	
3	–1.313 mV	–26 ±0.34	

Input R1, Channel 1

Number	DC Voltage	CURSOR dBm Reading	CURSOR Reading (dBm)
1	1.462V	+16 +0.25/–0.10	
2	–0.6208V	+9 +0.12/–0.10	
3	–1.313 mV	–26 ±0.34	

Input R2, Channel 1

Number	DC Voltage	CURSOR dBm Reading	CURSOR Reading (dBm)
1	–1.462V	+16 +0.25/–0.10	
2	–0.6208V	+9 +0.12/–0.10	
3	–1.313 mV	–26 ±0.34	

Input A, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	+10		+10.6 to +9.5
10	0		+0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Input B, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	+10		+10.6 to +9.5
10	0		+0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Input R1, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	+10		+10.6 to +9.5
10	0		+0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

Input R2, Channel 1

Attenuator Dial Setting	Input Power Level (dBm)	Cursor dBm Reading	Limits (dBm)
0	+10		+10.6 to +9.5
10	0		+0.6 to –0.5
20	–10		–9.4 to –10.5
30	–20		–19.4 to –20.5
40	–30		–29.3 to –30.6
50	–40		–39.3 to –40.7
60	–50		–49.0 to –50.9
60	–55		–53.9 to –56.1

SECTION 3
ADJUSTMENTS

CONTENTS

SECTION 3
ADJUSTMENTS

3-1 INTRODUCTION

This section contains the adjustment procedures for the 561. A performance verification test, using the DC Voltage Method, is also included at the end of paragraph 3-3. These procedures are usually done when out-of-specification conditions are noted in the Section 2, Performance Verificaton tests or as a result of subassembly/component repair or replacement.

3-2 RECOMMENDED TEST EQUIPMENT

Table 2-1 provides a listing of the recommended test equipment for performing the adjustment procedure. If the recommended items are not available, equipment with equivalent characteristics may be substituted.

3-3 ADJUSTMENT PROCEDURES

To perform the adjustment procedures, you must remove the top cover. See paragraph 4-2.1 for removal and replacement of the top cover.

1. Set up the test equipment as shown in Figure 3-1.
2. With the 561 off, press the POWER key on the 6647B and allow the self test to finish.
3. Press the RESET key on the 6647B.
4. Press the 561 POWER key and allow the self test to finish.

NOTE

Unless otherwise specified, the 561 is the instrument referred to in the following steps.

5. Press the SYSTEM RESET key.
6. Use the MENU up/down keys to highlight RESET.
7. Press the SELECT key.
8. Press the Channel 2 DISPLAY ON/OFF key to turn off the corresponding LED.
9. Press the Channel 1 MENU key.
10. Use the MENU up/down keys to highlight POWER.
11. Press the SELECT key.
12. Press the SELF TEST key. When the REMOTE LED comes on, immediately press and hold the STOP PRINT key. Release the STOP PRINT key when ENGINEERING MODE is displayed on the monitor screen. Ignore the FAILED TESTS message.

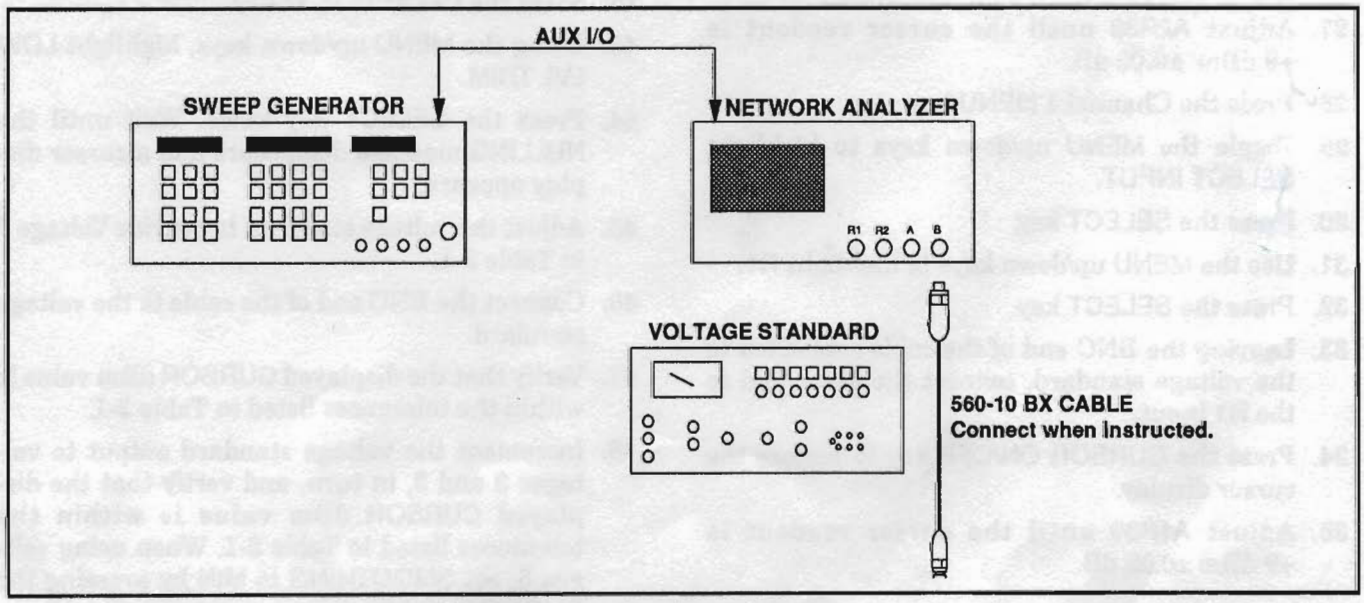

Figure 3-1. Test Equipment Setup for Adjustment Procedure

13. Press the SELECT key.
14. Simultaneously press the CALIBRATION and Channel 1 OFFSET/RESOLUTION keys until ENGINEERING MODE is highlighted on the right side of the monitor screen. It may take several attempts to do this (Figure 3-2).

CAUTION

Be careful not to disturb the front panel keys when making the following A1/A2 PCB adjustments.

15. Connect the 560-10BX cable to the A input. Leave the BNC end of the cable disconnected.
16. Adjust A2R62 for 0V ±0.2V, as read on the ENGINEERING MODE display (Figure 3-3).
17. Remove the cable from the A input and connect it to the B input.
18. Adjust A2R64 for 0V ±0.2V.
19. Remove the cable and connect it to the R1 input.
20. Adjust A1R62 for 0V ±0.2V.
21. Remove the cable and connect it to the R2 input.
22. Adjust A1R64 for 0V ±0.2V.
23. Press the CURSOR ON/OFF key to light the CURSOR LED. A cursor display should appear on the upper right side of the monitor screen.
24. Set the voltage standard for a –0.6208V output, which is equal to +9 dBm.
25. Connect the cable to the A input.
26. Connect the BNC end of the cable to the voltage standard.
27. Adjust A2R39 until the cursor readout is +9 dBm ±0.02 dB.
28. Press the Channel 1 MENU key.
29. Toggle the MENU up/down keys to highlight SELECT INPUT.
30. Press the SELECT key.
31. Use the MENU up/down keys to highlight R1.
32. Press the SELECT key.
33. Leaving the BNC end of the cable connected to the voltage standard, connect the other end to the R1 input.
34. Press the CURSOR ON/OFF key to restore the cursor display.
35. Adjust A1R39 until the cursor readout is +9 dBm ±0.02 dB.

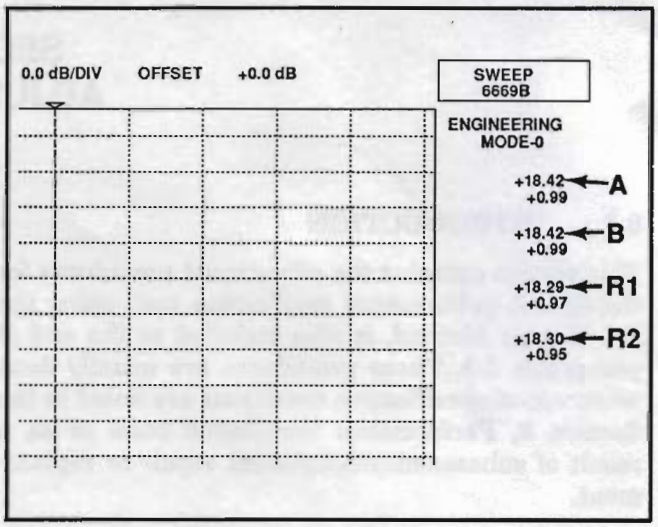

Figure 3-2. Monitor Display of Engineering Mode

NOTE

Steps 36 thru 56 constitute a performance verification test utilizing the DC Voltage Method.

36. Disconnect the BNC end of the cable from the voltage standard, and connect the other end to the A input.
37. Press the Channel 1 MENU key.
38. Toggle the MENU up/down keys to highlight SELECT INPUT.
39. Press the SELECT key.
40. Use the MENU up/down keys to highlight A.
41. Press the SELECT key.
42. Press the CALIBRATION key.
43. Using the MENU up/down keys, highlight LOW LVL TRIM.
44. Press the SELECT key twice. Wait until the NULLING message disappears and a cursor display appears.
45. Adjust the voltage standard to provide Voltage 1 in Table 3-1.
46. Connect the BNC end of the cable to the voltage standard.
47. Verify that the displayed CURSOR dBm value is within the tolerances listed in Table 3-1.
48. Increment the voltage standard output to voltages 2 and 3, in turn, and verify that the displayed CURSOR dBm value is within the tolerances listed in Table 3-1. When using voltage 3, set SMOOTHING to MIN by pressing the SMOOTHING key.

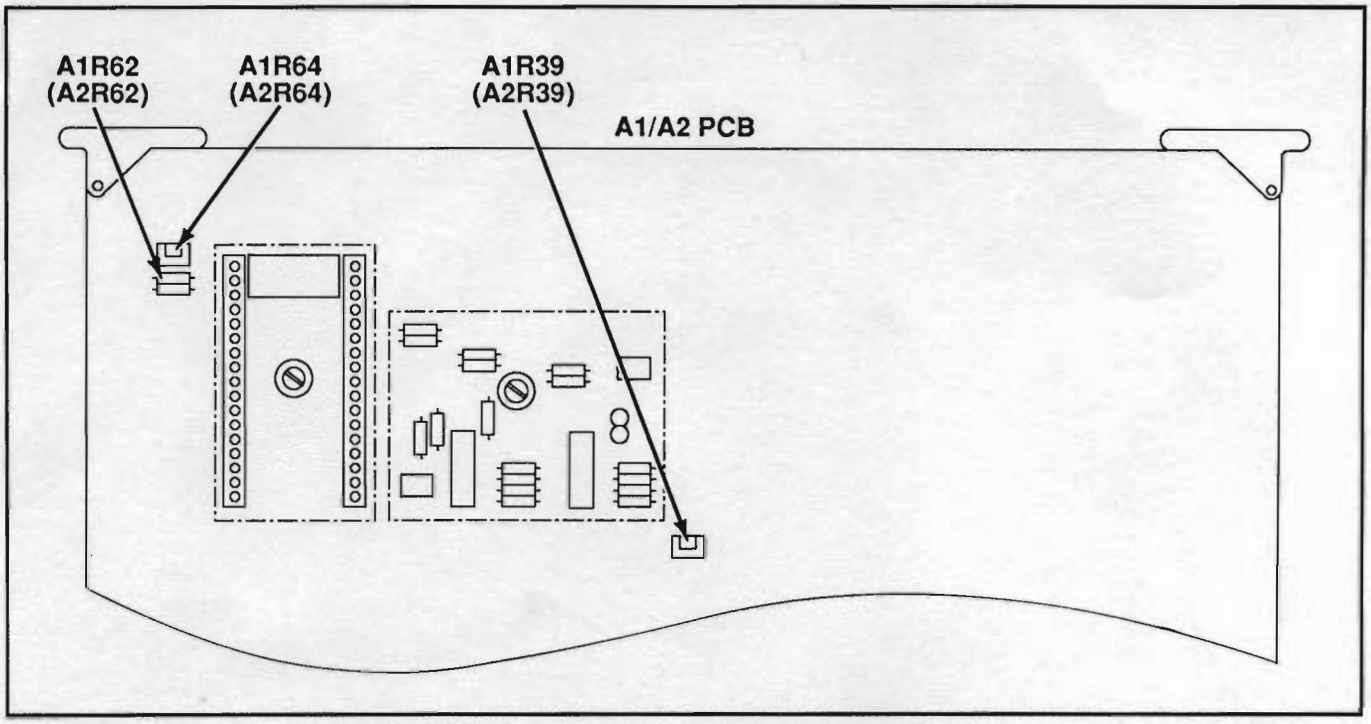

Figure 3-3. A1/A2 PCB Adjustments

49. Disconnect the BNC end of the cable from the voltage standard, and connect the other end to input B.
50. Press the Channel 1 MENU key.
51. Using the MENU up/down keys, highlight SELECT INPUT.
52. Press the SELECT key.
53. Using the MENU up/down keys, highlight B.
54. Press the SELECT key.
55. Repeat steps 42 thru 48 above.
56. Repeat steps 49 thru 55 for R1 and R2. In the procedure, substitute R1 and R2, respectively, for B.

Table 3-1. DC Voltage Chart

Number	DC Voltage	CURSOR dBm Reading
1	–1.462	+16, +0.25; 0.10
2	–0.6208	+9, +0.12; –0.10
3	–1.313 mV	–26, ±0.34

3-4 SWEEP RAMP AMPLIFIER GAIN ADJUSTMENT

This procedure covers adjustment of the Sweeper Interface (A4) PCB Assembly, using a 561 chassis and a 561 Extender PCB. This procedure is only required after repair or replacement of the A4 PCB.

1. Connect a function generator to an oscilloscope. On the function generator, select a triangular waveform and a frequency of 100 Hz. Set the amplitude to 13V peak to peak while monitoring the signal on the oscilloscope. Adjust the offset so that the upper limit of the signal is +12V and the lower limit is –1V.
2. Without altering any of its settings, disconnect the function generator from the oscilloscope and connect it to the BNC connector marked HORIZONTAL INPUT on the rear panel of the 561 chassis.
3. Attach a x10 probe to the oscilloscope. Connect the probe to TP2 and the ground clip to TP6 (0V).
4. The oscilloscope should show a triangular wave of 100 Hz at ≈10 V_{p-p} amplitude. Adjust R10 until the upper limit of the waveform is exactly 10V above the 0V level. This completes the adjustment and verification of the Sweep Ramp circuit.

SECTION 4
DISASSEMBLY AND REPAIR PROCEDURES

CONTENTS

SECTION 4
DISASSEMBLY AND REPAIR

4-1 INTRODUCTION

The disassembly procedures in this section show how to gain access to major instrument parts for troubleshooting or maintenance.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. The instrument must be turned off and the line cord must be disconnected before removing any covers or panels. Repair procedures should only be performed by service persons who are fully aware of the potential hazards.

4-2 DISASSEMBLY PROCEDURES

All procedures in this section should be done with the top and bottom covers and side panels removed. Removal procedures for the covers and panels are described in paragraph 4-2.1.

4-2.1 Rear Feet, Covers, and Side Panels

1. Turn off the power. Disconnect all external cables.
2. Turn the instrument on its side and remove two of the rear feet with a pozidriv 2 screwdriver.
3. Turn the instrument on its other side and remove the other two feet.
4. Slide the top and bottom covers and the side panels off the instrument.
5. To replace, reverse the procedure described in steps 1 thru 4.

4-2.2 Bottom Feet

1. On the inside of the bottom cover, use a phillips-1 screwdriver to remove the screw for each foot being replaced.
2. To replace, fit each peg in the corresponding opening and reverse the procedure described in step 1.

4-2.3 Front Panel Assembly

The front panel assembly consists of the front panel, the Switch Mounting (A11) PCB, the Front Panel (A13) PCB, and the input connectors. Refer to Figure 4-1 for removal and replacement of this assembly.

a. Front Panel

1. Remove the cable connectors at A1P1, A1P2, A2P1, A2P2, A9P2, and A13P1.
2. Using a phillips-1 screwdriver, remove the two screws fastening the front panel cables to the side of the card cage.
3. Using a ball hex wrench, remove the eight hex screws from the inside of the front panel and pull the panel out of the instrument.
4. To replace, reverse the procedure described in steps 1 thru 3.

b. A11 Switch Mounting PCB

1. Remove the front panel as described in paragraph 4-2.3a.
2. Using a .035 hex key, loosen the two hex screws in the intensity knob and remove the knob.
3. Using a phillips-1 screwdriver, remove the three screws from the A11 PCB.
4. Pull the A11 PCB out from the assembly and remove the connector at A11P1.
5. To replace, reverse the procedure described in steps 1 thru 4.

c. A13 Front Panel PCB

1. Remove the front panel as described in paragraph 4-2.3a.
2. Remove the cable connector at A13P2.
3. Using a phillips-1 screwdriver, loosen one or more of the screws that hold the A11 PCB, and push the PCB up slightly to remove the connector at A11P1.
4. Using a phillips-1 screwdriver, remove the eight screws from the A13 PCB and pull it out of the assembly.
5. To replace, reverse the procedure described in steps 1 thru 4.

NOTE

Be sure to route the A11P1 connector wires above the corner screw of the A13 PCB to avoid damaging the wires during reassembly.

d. Input Connectors

Each input connector assembly (connector and attached assembly) is a replaceable item.

1. Remove the front panel as described in paragraph 4-2.3a.
2. Unfasten the cover plate by removing the four screws with a phillips-1 screwdriver.
3. Using a 3/16" hex nut driver, remove the nuts and washers from the connector(s) being replaced.
4. Lift the solder lug from the integral threaded stud and remove the connector and attached cable from the front panel.
5. To replace, reverse the procedure described in steps 1 thru 4.

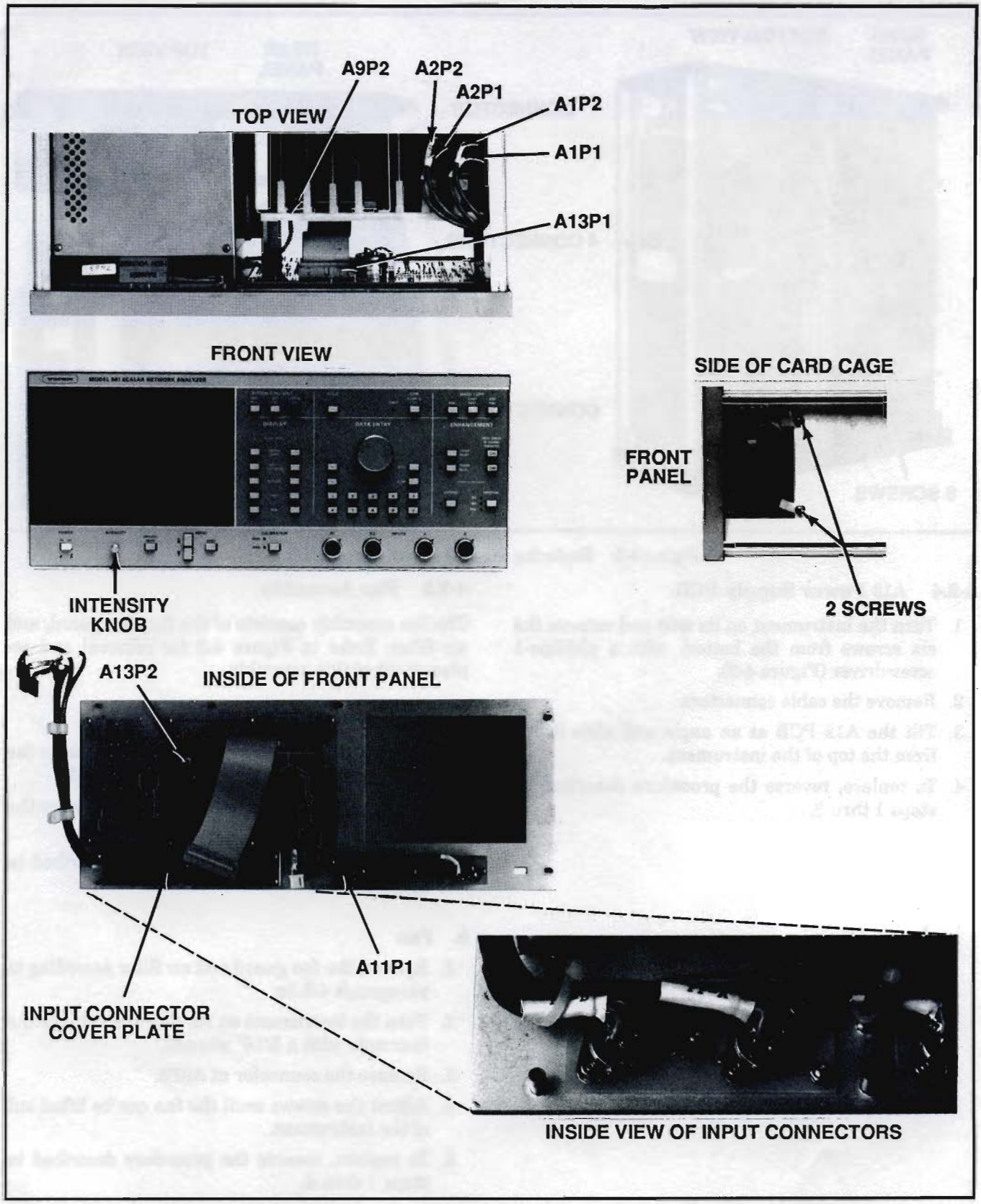

Figure 4-1. Replacing the Front Panel Assembly

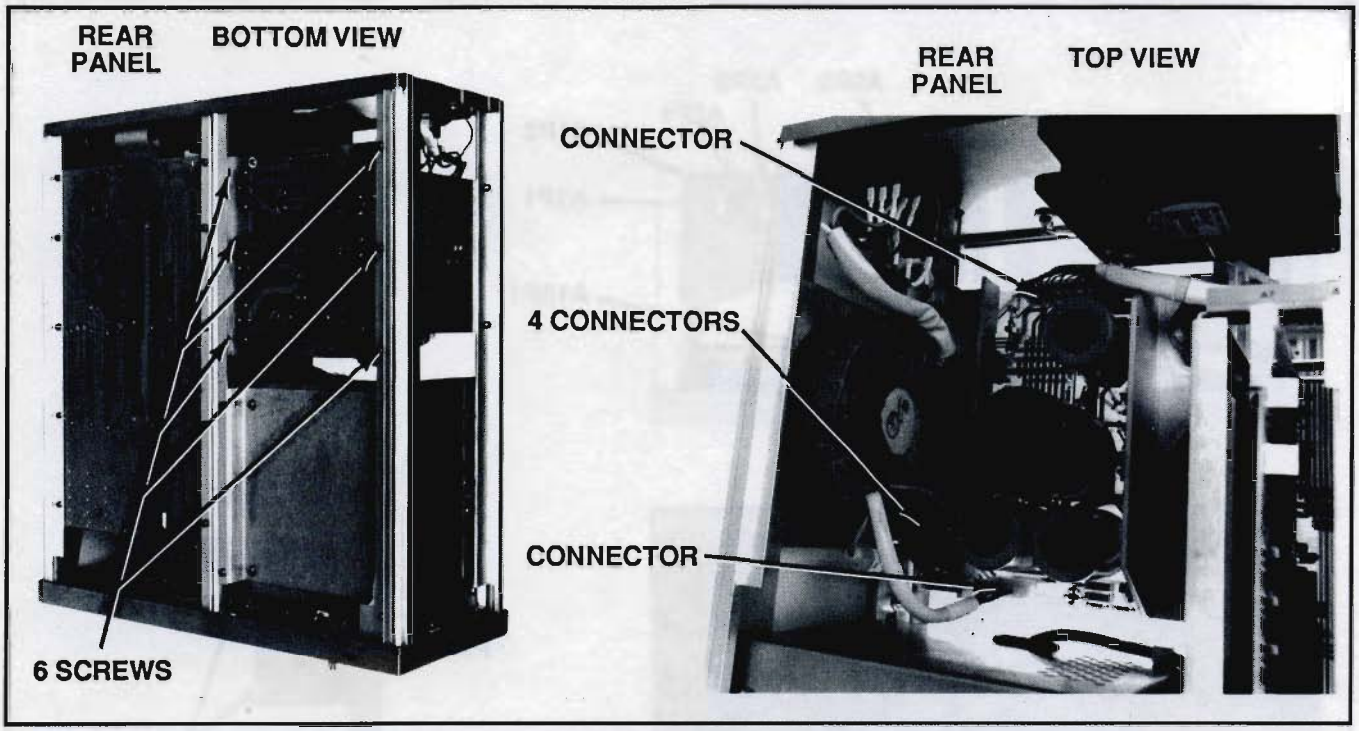

Figure 4-2. Replacing the A12 Power Supply PCB

4-2.4 A12 Power Supply PCB

1. Turn the instrument on its side and remove the six screws from the bottom with a phillips-1 screwdriver (Figure 4-2).
2. Remove the cable connectors.
3. Tilt the A12 PCB at an angle and slide it out from the top of the instrument.
4. To replace, reverse the procedure described in steps 1 thru 3.

4-2.5 Fan Assembly

The fan assembly consists of the fan, fan guard, and air filter. Refer to Figure 4-3 for removal and replacement of this assembly.

a. Fan Guard and Air Filter

1. Use a 5/16" wrench or nut driver to remove the four nuts on the outside of the fan guard.
2. Lift the fan guard off the screws and remove the air filter.
3. To replace, reverse the procedure described in steps 1 and 2.

b. Fan

1. Remove the fan guard and air filter according to paragraph 4-2.5a.
2. Turn the instrument on its side and remove the four nuts with a 5/16" wrench.
3. Remove the connector at A9P5.
4. Adjust the screws until the fan can be lifted out of the instrument.
5. To replace, reverse the procedure described in steps 1 thru 4.

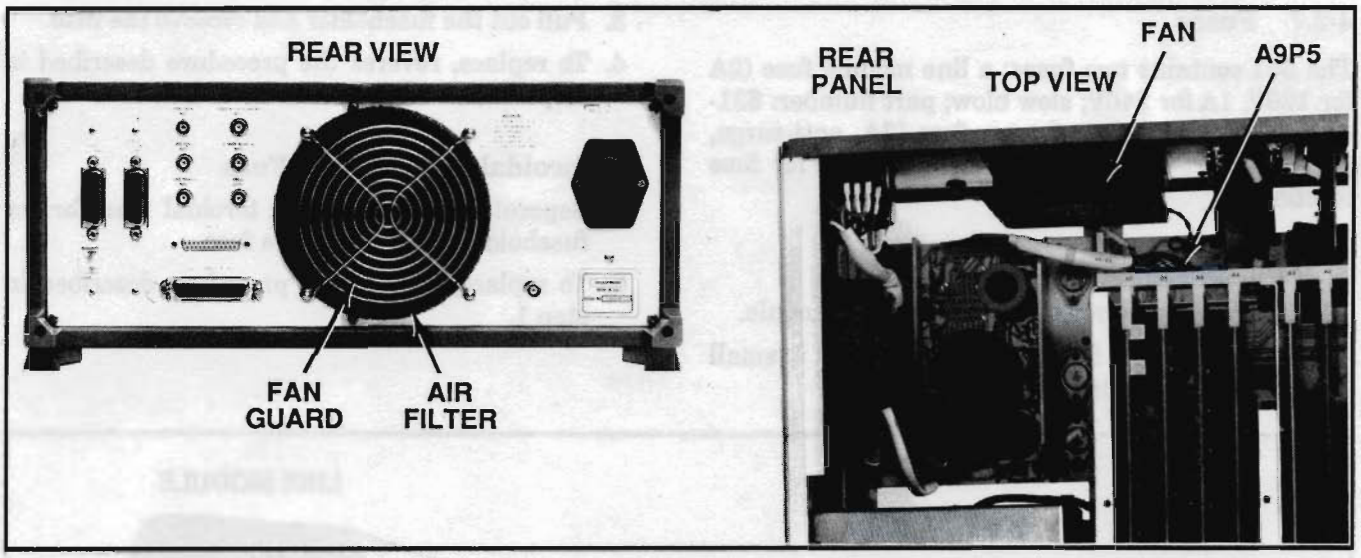

Figure 4-3. Replacing the Fan Assembly

4-2.6 Line Module

1. Remove the power cord from the line module (Figure 4-4).
2. Remove the two screws on the outside of the line module with a phillips-1 screwdriver.
3. Remove the ten connectors shown in Figure 4-4. Do not remove the grounding connector, since it is soldered to the line module.
4. Using a phillips-1 screwdriver, remove the screw connecting the green/white grounding wire to the chassis.
5. Pull the line module out of the instrument.
6. To replace, reverse the procedure described in steps 1 thru 4. Refer to Figure 6K-2 for wiring information, if necessary.

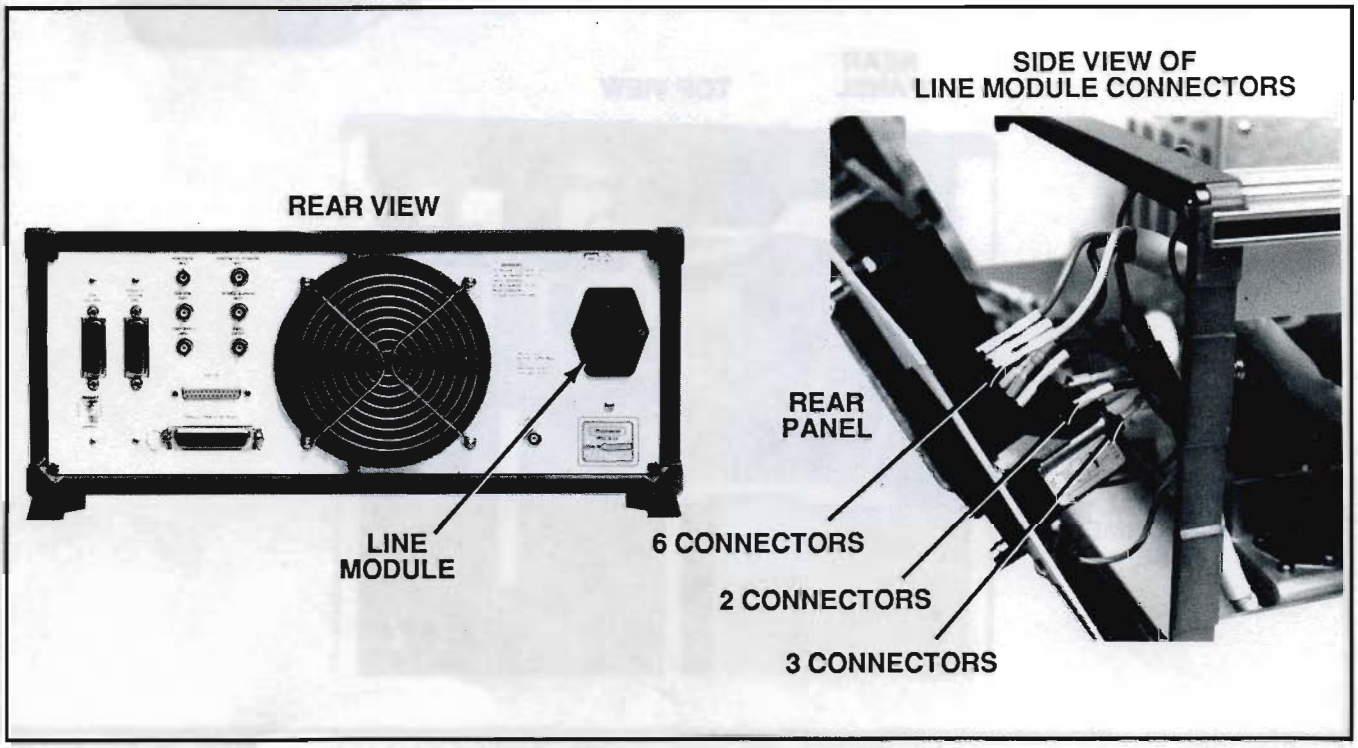

Figure 4-4. Replacing the Line Module

4-2.7 Fuses

The 561 contains two fuses; a line module fuse (2A for 120V, 1A for 240V; slow blow; part number: 631-4) and a toroidal transformer fuse (7A, anti-surge, part number: 631-56). Refer to Figure 4-5 for fuse locations.

a. Line Module Fuse

1. Remove the power cord from the line module.
2. Flip open the fuseholder cover with a small flathead screwdriver.
3. Pull out the fuseholder and remove the fuse.
4. To replace, reverse the procedure described in steps 1 thru 3.

b. Toroidal Transformer Fuse

1. Seperate the ends of the toroidal transformer fuseholder and remove the fuse.
2. To replace, reverse the procedure described in step 1.

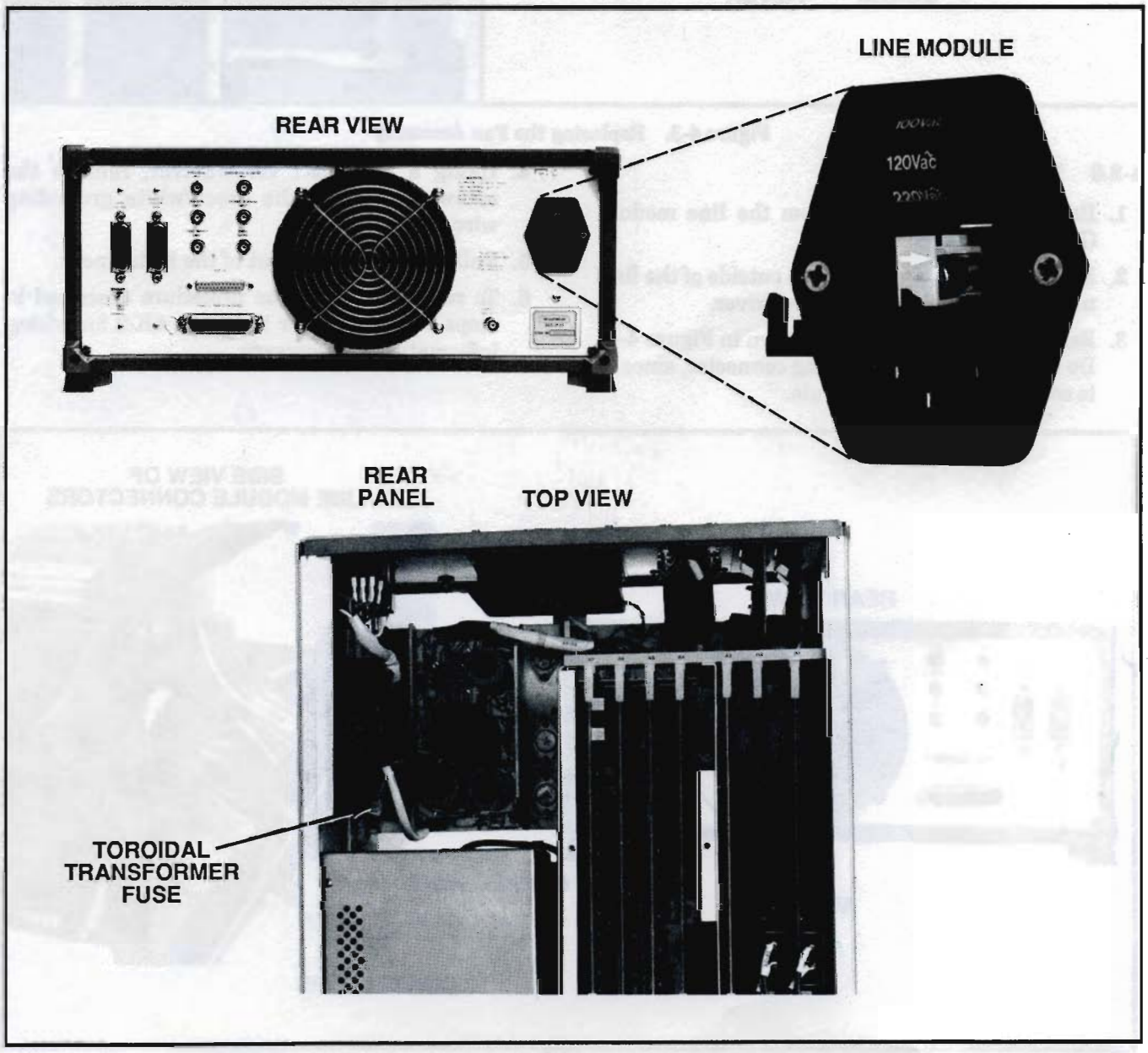

Figure 4-5. Locations of the Line Module and Toroidal Transformer Fuses

4-2.8 GPIB Assembly: A8 System GPIB PCB and A10 Dedicated GPIB PCB

1. Using a phillips-1 screwdriver, remove the four screws that attach the GPIB assembly to the rear panel (Figure 4-6).
2. Remove the connectors at A9P9 and A9P10, and lift the GPIB assembly from the instrument.
3. Using a flathead screwdriver, remove the two screws fastening the A8P1 connector and connector plate to the assembly bracket, and remove the A8 PCB. Follow the same procedure when removing the A10 PCB.
4. To replace, reverse the procedure described in steps 1 thru 3.

Reassembly Hint

It is easier to replace the A8 PCB with the A10 PCB removed from the bracket.

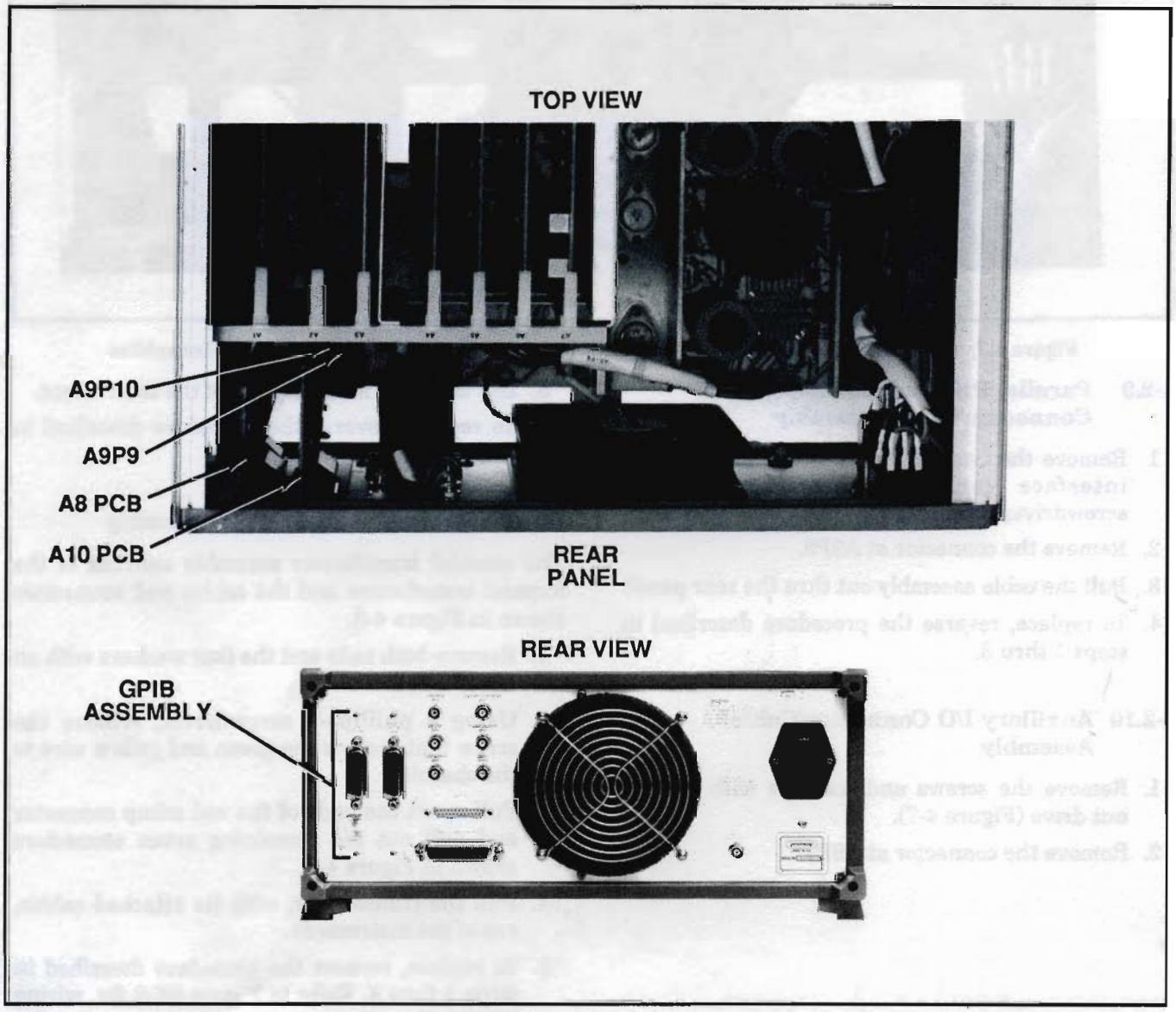

Figure 4-6. Replacing the GPIB (A8 and A10 PCBs) Assembly

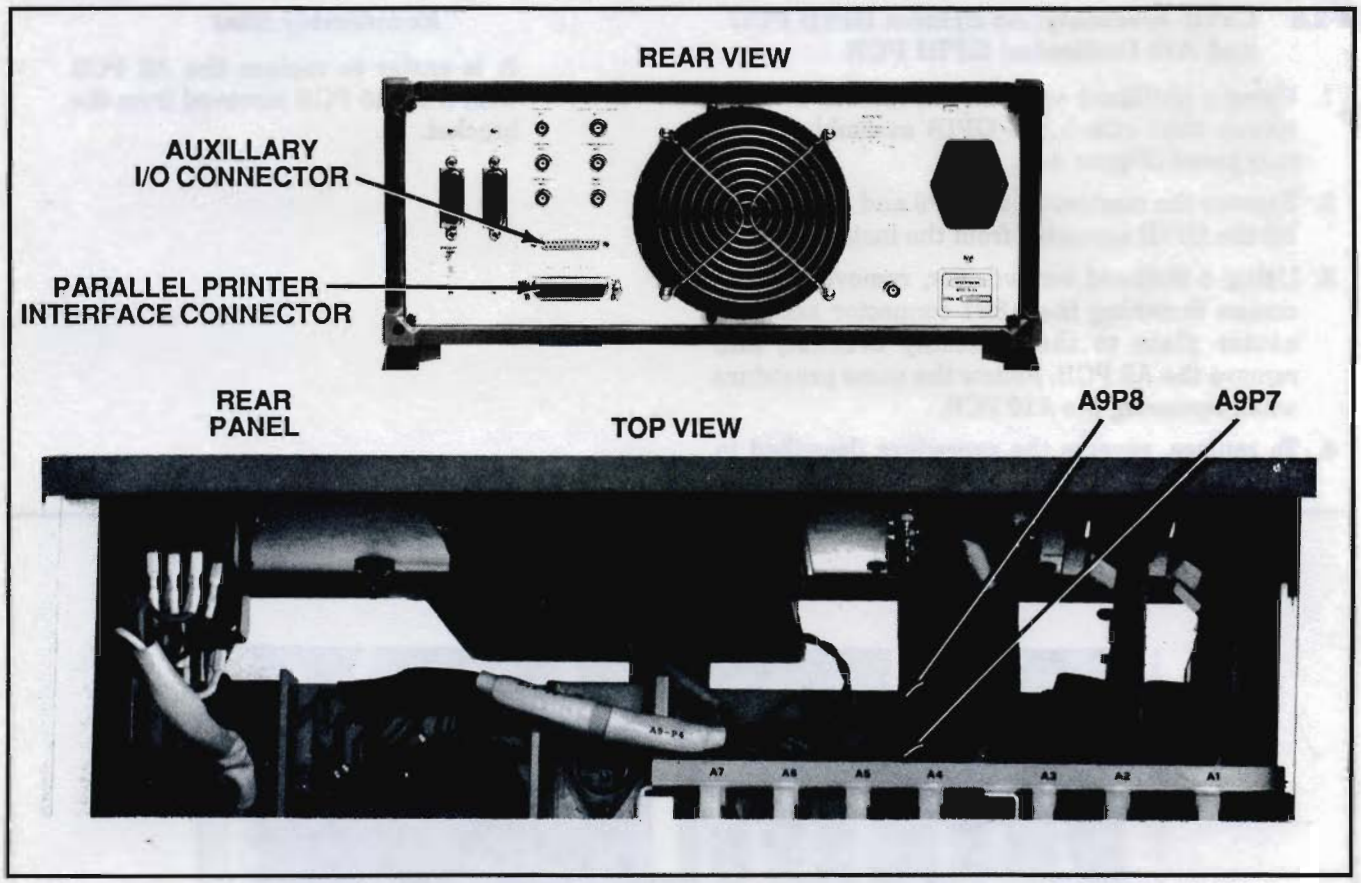

Figure 4-7. Replacing the Parallel Printer Interface and Auxillary I/O Connector/Cable Assemblies

4-2.9 Parallel Printer Interface Connector/Cable Assembly

1. Remove the two screws in the parallel printer interface connector with a phillips-1 screwdriver (Figure 4-7).
2. Remove the connector at A9P8.
3. Pull the cable assembly out thru the rear panel.
4. To replace, reverse the procedure described in steps 1 thru 3.

4-2.10 Auxillary I/O Connector/Cable Assembly

1. Remove the screws and washers with a 3/16" nut drive (Figure 4-7).
2. Remove the connector at A9P7.
3. Lift the cable assembly out of the instrument.
4. To replace, reverse the procedure described in steps 1 thru 3.

4-2.11 Toroidal Transformer Assembly

The toroidal transformer assembly consists of the toroidal transformer and the cables and connectors shown in Figure 4-8.

1. Remove both nuts and the four washers with an 11/32" nut driver.
2. Using a phillips-1 screwdriver, remove the screw that fastens the green and yellow wire to the chassis.
3. Pull apart the ends of the red crimp connector and pull out the remaining seven connectors shown in Figure 4-8.
4. Pull the transformer, with its attached cables, out of the instrument.
5. To replace, reverse the procedure described in steps 1 thru 4. Refer to Figure 6K-2 for wiring information, if necessary.

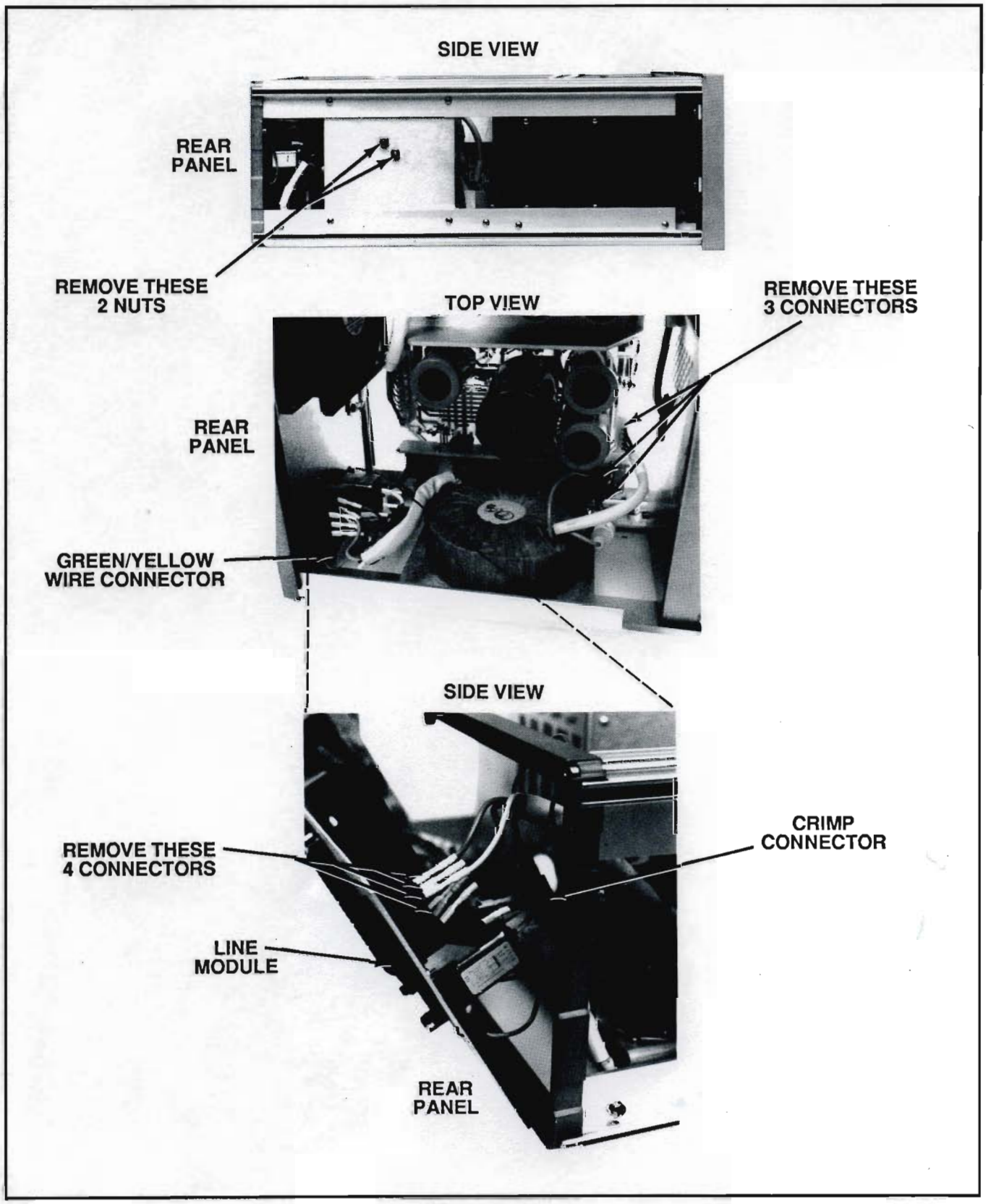

Figure 4-8. Replacing the Toroidal Transformer Assembly

SECTION 5
PARTS LISTS

CONTENTS

SECTION 5
PARTS LISTS

5-1 INTRODUCTION

This section provides parts lists for the 561 Scalar Network Analyzer. The parts lists are divided into two groups:

- Printed circuit board (PCB) parts (Tables 5-4 thru 5-15)
- Major assembly parts (Figures 5-1 thru 5-4)

5-2 PARTS-ORDERING INFORMATION

Parts may be ordered from your local WILTRON representative or directly from the factory.

WILTRON Company
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: 408-778-2000
TWX: 285227 WILTRON MH
FAX: 408-778-0239

When ordering, give complete information including the model and serial number of the instrument, the full part description, the WILTRON part number, and the quantity required.

5-3 ABBREVIATIONS

Common abbreviations used in the parts list descriptions are defined in Table 5-1.

5-4 ORGANIZATION OF PARTS LISTS

Table 5-2 lists the location of all PCBs and major assembly groups.

5-5 EXCHANGE ASSEMBLIES

Table 5-3 lists the replaceable assemblies and their WILTRON part numbers.

Table 5-1. Common Abbreviations Used in the Parts List

Abbreviation	Description	Abbreviation	Description
A	Ampere, Assembly	N	Not Assigned
B	Fan	P	Pin, Plug
C	Capacitor	PCB	Printed Circuit Board
CC	Carbon Composition	Q	Transistor
CER	Ceramic	R	Resistor
CR	Diode	RN	Resistor Network
DS	Display Indicator	S	Switch
E	Miscellaneous Electrical Part	SI	Silicon
F	Female	SW	Switch
FF	Flip Flop	T	Transformer
FXD	Fixed	TANT	Tantalum
HDR	Header	TP	Test Point
J	Jack	U	Integrated Circuit
K	Kilo (10^3), Relay	UF	Micro Farad
L	Inductor	UH	Micro Henry
LCD	Liquid Crystal Display	V	Volt
LED	Light Emitting Diode	VR	Voltage Regulator
M	Male, Meg- (10^6)	W	Watt, Wire Jumper
MF	Metal Film	Y	Crystal
MH	Milli Henry (mH)		

Table 5-2. Organization of Parts Lists

Table/Figure	PCB Assembly Name	Wiltron Part Number	Page
	Printed Circuit Boards (PCBs)		
Table 5-4	A1/A2 Signal Channel Amplifier	561-D-32512-3	5-5
Table 5-5	A3 Signal Channel Interface	561-D-32513-3	5-8
Table 5-6	A4 Sweeper Interface	561-D-32514-3	5-10
Table 5-7	A5 CPU	561-D-32515-3	5-12
Table 5-8	A6 Text and Graphics Processor	561-D-32516-3	5-13
Table 5-9	A7 Video Display Processor	561-D-32517-3	5-14
Table 5-10	A8 System GPIB	561-D-32518-3	5-16
Table 5-11	A10 Dedicated GPIB	561-D-32520-3	5-16
Table 5-12	A9 Motherboard	561-D-32519-3	5-16
Table 5-13	A11 Switch Mounting	561-D-32523-3	5-28
Table 5-14	A12 Power Supply	561-D-32521-3	5-17
Table 5-15	A13 Front Panel	561-D-32511-3	5-18
	Major Assembly Illustrated Parts		
Figure 5-1	Case Assembly	561-D-32501-3	5-19
Figure 5-2	Front Panel Assembly	561-D-32502-3	5-21
Figure 5-3	Rear Panel	561-D-32503-3	5-22
Figure 5-4	GPIB Assembly	561-D-32507-3	5-23

Table 5-3. Exchange Assemblies

QTY	DESCRIPTION	WILTRON PART NO.
1	A1/A2 Signal Channel PC Assembly	561-D-32512-3
1	A3 Signal Interface PC Assembly	561-D-32513-3
1	A4 Sweeper Interface PC Assembly	561-D-32514-3
1	A5 CPU PC Assembly	561-D-32515-3
1	A6 Graphics Processor PC Assembly	561-D-32516-3
1	A7 Video Display Processor Assembly	561-D-32517-3
1	A8 GPIB PC Assembly	561-D-32518-3
1	A10 Dedicated GPIB PC Assembly	561-D-32520-3
1	A12 Power Supply Assembly	561-D-32521-3
1	A13 Front Panel Assembly	561-D-32511-3
1	Monitor Assembly	561-D-32508

Table 5-4. A1/A2 Signal Channel Amp (1 of 5)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	223-150	1	CAPACITOR,FXD,MICA,150PF,5%
C2	230-30	11	CAPACITOR,FXD,CER,1000PF,+80/-20%
C3	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C4	250-42		CAPACITOR,FXD,TANT,10µF,10%
C5	250-42	40	CAPACITOR,FXD,TANT,10µF,10%
C6	250-42		CAPACITOR,FXD,TANT,10µF,10%
C7	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C8	250-42		CAPACITOR,FXD,TANT,10µF,10%
C9	250-42		CAPACITOR,FXD,TANT,10µF,10%
C10	250-42		CAPACITOR,FXD,TANT,10µF,10%
C11	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C12	250-42		CAPACITOR,FXD,TANT,10µF,10%
C13	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C14	250-42		CAPACITOR,FXD,TANT,10µF,10%
C15	250-42		CAPACITOR,FXD,TANT,10µF,10%
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	250-42		CAPACITOR,FXD,TANT,10µF,10%
C18	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C19	250-42		CAPACITOR,FXD,TANT,10µF,10%
C20	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C21	250-42		CAPACITOR,FXD,TANT,10µF,10%
C22	250-42		CAPACITOR,FXD,TANT,10µF,10%
C23	250-42		CAPACITOR,FXD,TANT,10µF,10%
C24	250-42		CAPACITOR,FXD,TANT,10µF,10%
C25	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C26	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C27	250-42		CAPACITOR,FXD,TANT,10µF,10%
C28	250-42		CAPACITOR,FXD,TANT,10µF,10%
C29	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C30	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C31			NOT ASSIGNED
C32	230-87	2	CAPACITOR,FIXED,PEST,1.0µF
C33	210-38	2	CAPACITOR,FXD,PEST,0.022µF
C34	210-38		CAPACITOR,FXD,PEST,0.022µF
C35	230-87		CAPACITOR,FIXED,PEST,1.0µF
C36	210-20	1	CAPACITOR,FXD,PEST,0.01µF,10%
C37	250-42		CAPACITOR,FXD,TANT,10µF,10%
C38	250-42		CAPACITOR,FXD,TANT,10µF,10%
C39	250-42		CAPACITOR,FXD,TANT,10µF,10%
C40	250-42		CAPACITOR,FXD,TANT,10µF,10%
C41	250-42		CAPACITOR,FXD,TANT,10µF,10%
C42	250-42		CAPACITOR,FXD,TANT,10µF,10%
C43	250-42		CAPACITOR,FXD,TANT,10µF,10%
C44	250-42		CAPACITOR,FXD,TANT,10µF,10%
C45	230-37	21	CAPACITOR,FXD,CER,0.1µF,20%
C46	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C47	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C48	250-42		CAPACITOR,FXD,TANT,10µF,10%
C49	250-42		CAPACITOR,FXD,TANT,10µF,10%
C50	250-42		CAPACITOR,FXD,TANT,10µF,10%
C51	250-42		CAPACITOR,FXD,TANT,10µF,10%
C52	250-42		CAPACITOR,FXD,TANT,10µF,10%
C53	250-42		CAPACITOR,FXD,TANT,10µF,10%
C54			NOT ASSIGNED
C55			NOT ASSIGNED
C56	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C57	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C58	250-42		CAPACITOR,FXD,TANT,10µF,10%
C59	250-42		CAPACITOR,FXD,TANT,10µF,10%
C60	230-37		CAPACITOR,FXD,CER,0.1µF,20%

Table 5-4. A1/A2 Signal Channel Amp (2 of 5)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C61			NOT ASSIGNED
C62	250-42		CAPACITOR,FXD,TANT,10µF,10%
C63	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C64	250-42		CAPACITOR,FXD,TANT,10µF,10%
C65	250-42		CAPACITOR,FXD,TANT,10µF,10%
C66	223-10	3	CAPACITOR,FXD,MICA,10PF,5%
C67	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C68	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C69	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C70	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
C71			NOT ASSIGNED
C72			NOT ASSIGNED
C73	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C74	250-42		CAPACITOR,FXD,TANT,10µF,10%
C75	250-42		CAPACITOR,FXD,TANT,10µF,10%
C76	250-42		CAPACITOR,FXD,TANT,10µF,10%
C77	223-10		CAPACITOR,FXD,MICA,10PF,5%
C78			NOT ASSIGNED
C79	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C80	250-42		CAPACITOR,FXD,TANT,10µF,10%
C81	223-10		CAPACITOR,FXD,MICA,10PF,5%
C82	223-560	1	CAPACITOR,FXD,CER,560PF,10%
C83	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C84	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C85	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C86	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C87	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C88	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C89	250-57	1	CAPACITOR,FXD,TANT,150µF,10%
C90	230-33	1	CAPACITOR,FXD,CER,2000PF,20%
C91	230-30		CAPACITOR,FXD,CER,1000PF,+80/-20%
CR1	10-60	14	DIODE,RECTIFIER,IN4148,75V
CR2	10-60		DIODE,RECTIFIER,IN4148,75V
CR3	10-60		DIODE,RECTIFIER,IN4148,75V
CR4	10-60		DIODE,RECTIFIER,IN4148,75V
CR5	10-60		DIODE,RECTIFIER,IN4148,75V
CR6	10-60		DIODE,RECTIFIER,IN4148,75V
CR7	10-60		DIODE,RECTIFIER,IN4148,75V
CR8	10-60		DIODE,RECTIFIER,IN4148,75V
CR9	10-1N752A	1	DIODE,ZENER,1N752A,5.6V,5%
CR10	10-60		DIODE,RECTIFIER,IN4148,75V
CR11	10-60		DIODE,RECTIFIER,IN4148,75V
CR12	10-1N964B	2	DIODE,ZENER,1N964B,13V,5%
CR13	10-1N964B		DIODE,ZENER,1N964B,13V,5%
CR14	10-60		DIODE,RECTIFIER,IN4148,75V
CR15	10-60		DIODE,RECTIFIER,IN4148,75V
CR16	10-60		DIODE,RECTIFIER,IN4148,75V
CR17	10-60		DIODE,RECTIFIER,IN4148,75V
J1	551-173	2	CONNECTOR,HDR HSNG,PC MNT
J2	551-173		CONNECTOR,HDR HSNG,PC MNT
L1	310-116	3	INDUCTOR,FXD,1.9µH
L2	310-116		INDUCTOR,FXD,1.9µH
L3	310-116		INDUCTOR,FXD,1.9µH
P1	552-5	1	CONNECTOR,ERO,PLUG
P2	551-571	1	CONNECTOR,HEADER,1ROW
Q1	20-2N4410	2	TRANSISTOR,NPN,2N4410,SI
Q2	20-2N4410		TRANSISTOR,NPN,2N4410,SI
R1	110-10K-1	20	RESISTOR,FXD,MF,10K,1%,0.25W
R2	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R3	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W

Table 5-4. A1/A2 Signal Channel Amp (3 of 5)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R4	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R5	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R6	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R7	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R8	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R9	110-21.5K-1	4	RESISTOR,FXD,MF,21.5K,1%,0.25W
R10	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R11	110-20K-1	8	RESISTOR,FXD,MF,20K,1%,0.25W
R12	110-18.7K-1	2	RESISTOR,FXD,MF,18.7K,1%,0.25W
R13	110-1.87K-1	3	RESISTOR,FXD,MF,1.87K,1%,0.25W
R14	110-187-1	2	RESISTOR,FXD,MF,187,1%,0.25W
R15	156-200-C	1	RESISTOR,TRIM,CER,200
R16	110-19.6-1	1	RESISTOR,FXD,MF,19.6,1%,0.25W
R17	110-30.1-1	1	RESISTOR,FXD,MF,30.1,1%,0.25W
R18	110-187-1		RESISTOR,FXD,MF,187,1%,0.25W
R19	110-1.87K-1		RESISTOR,FXD,MF,1.87K,1%,0.25W
R20	110-18.7K-1		RESISTOR,FXD,MF,18.7K,1%,0.25W
R21	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R22	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R23	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R24	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R25	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R26	110-5.11K-1	3	RESISTOR,FXD,MF,5.11K,1%,0.25W
R27	110-196-1	2	RESISTOR,FXD,MF,196,1%,0.25W
R28	110-21.5K-1		RESISTOR,FXD,MF,21.5K,1%,0.25W
R29	110-21.5K-1		RESISTOR,FXD,MF,21.5K,1%,0.25W
R30	110-100-1	8	RESISTOR,FXD,MF,100,1%,0.25W
R31	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R32	110-1K-1	15	RESISTOR,FXD,MF,1K,1%,0.25W
R33	110-21.5K-1		RESISTOR,FXD,MF,21.5K,1%,0.25W
R34	157-20K-A	1	RESISTOR,TRIM,CER,20K,10%,18T
R35	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R36	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R37	110-7.5K-1	1	RESISTOR,FXD,MF,7.5K,1%,0.25W
R38	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R39	156-2K-C	1	RESISTOR,TRIM,CER,2K
R40	157-10K-A	1	RESISTOR,TRIM,CER,10K
R41	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R42	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R43	110-42.2K-1	1	RESISTOR,FXD,MF,42.2K,1%,0.25W
R44	110-53.6K-1	1	RESISTOR,FXD,MF,53.6K,1%,0.25W
R45	110-10.5K-1	2	RESISTOR,FXD,MF,10.5K,1%,0.25W
R46	156-200-A	1	RESISTOR,TRIM,CER,200
R47	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R48	110-15.4K-1	1	RESISTOR,FXD,MF,15.4K,1%,0.25W
R49	110-95.3K-1	1	RESISTOR,FXD,MF,95.3K,1%,0.25W
R50	156-10K-A	1	RESISTOR,TRIM,CER,10K
R51	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R52	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R53	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R54	110-5.11K-1		RESISTOR,FXD,MF,5.11K,1%,0.25W
R55	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R56	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R57	110-196-1		RESISTOR,FXD,MF,196,1%,0.25W
R58			NOT ASSIGNED
R59	110-1.87K-1		RESISTOR,FXD,MF,1.87K,1%,0.25W
R60	110-825K-1	4	RESISTOR,FXD,MF,825K,1%,0.25W
R61	110-825K-1		RESISTOR,FXD,MF,825K,1%,0.25W
R62	156-200K-C	2	RESISTOR,TRIM,CER,200K
R63	110-825K-1		RESISTOR,FXD,MF,825K,1%,0.25W

Table 5-4. A1 or A2 Signal Channel Amp (4 of 5)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R64	156-200K-C		RESISTOR,TRIM,CER,200K
R65	110-825K-1		RESISTOR,FXD,MF,825K,1%,0.25W
R66	110-100K-1	2	RESISTOR,FXD,MF,100K,1%,0.25W
R67	110-511-1	2	RESISTOR,FXD,MF,511,1%,0.25W
R68	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R69	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R70	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R71	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R72	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R73	110-511-1		RESISTOR,FXD,MF,511,1%,0.25W
R74			NOT ASSIGNED
R75			NOT ASSIGNED
R76			NOT ASSIGNED
R77			NOT ASSIGNED
R78			NOT ASSIGNED
R79			NOT ASSIGNED
R80			NOT ASSIGNED
R81			NOT ASSIGNED
R82	110-51.1-1	1	RESISTOR,FXD,MF,51.1,1%,0.25W
R83	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R84	110-20K-1		RESISTOR,FXD,MF,20K,1%,0.25W
R85	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R86	110-5.11K-1		RESISTOR,FXD,MF,5.11K,1%,0.25W
R87	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R88	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R89	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R90	110-3.83K-1	1	RESISTOR,FXD,MF,3.83K,1%,0.25W
R91	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R92	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R93	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R94	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R95	110-3.32K-1	2	RESISTOR,FXD,MF,3.32K,1%,0.25W
R96	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R97	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R98	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R99			NOT ASSIGNED
R100	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R101	110-10.5K-1		RESISTOR,FXD,MF,10.5K,1%,0.25W
R102	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R103	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R104	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R105	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R106	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R107	110-110K-1	2	RESISTOR,FXD,MF,110K,1%,0.25W
R108	101-1M-5	2	RESISTOR,FXD,CC,1M,5%,0.25W
R109	158-15	2	RESISTOR,TRIM,CER,100K
R110	101-1M-5		RESISTOR,FXD,CC,1M,5%,0.25W
R111	110-110K-1		RESISTOR,FXD,MF,110K,1%,0.25W
R112	158-15		RESISTOR,TRIM,CER,100K
RN1	123-1K	1	RESISTOR,NETWORK,1K
TP1	702-17	13	TERMINAL EYELET
TP2	702-17		TERMINAL EYELET
TP3	702-17		TERMINAL EYELET
TP4	702-17		TERMINAL EYELET
TP5	702-17		TERMINAL EYELET
TP6	702-17		TERMINAL EYELET
TP7	702-17		TERMINAL EYELET
TP8	702-17		TERMINAL EYELET
TP9	702-17		TERMINAL EYELET
TP10	702-17		TERMINAL EYELET

Table 5-4. A1 or A2 Signal Channel Amp (5 of 5)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
TP11	702-17		TERMINAL EYELET
TP12	702-17		TERMINAL EYELET
TP13	702-17		TERMINAL EYELET
U1	54-596	1	AD625JN INST AMPLIFIER
U2	54-597	1	IC,ANALOGUE SWITCH,AD7502JN
U3	54-595	2	IC,OP-AMP,OP-27GP
U4	54-595		IC,OP-AMP,OP-27GP
U5	54-208	3	IC,ANALOG SWITCH,DG211
U6	54-714	1	IC,OP-AMP,AD712KN
U7	54-593	1	IC,D/A,AD7533LN,10BIT,BINARY
U8	54-43	4	IC,TTL,74LS174,HEX,D FLIP FLOP
U9	54-43		IC,TTL,74LS174,HEX,D FLIP FLOP
U10	54-43		IC,TTL,74LS174,HEX,D FLIP FLOP
U11	54-208		IC,ANALOG SWITCH,DG211
U12	54-208		IC,ANALOG SWITCH,DG211
U13	54-204	1	IC,OP AMP,LF398
U14	54-74LS138	1	IC,TTL,74LS138,3 TO 8 DECODER
U15	54-41	1	IC,TTL,74LS374,OCTAL,D FLIP FLOP
U16	54-43		IC,TTL,74LS174,HEX,D FLIP FLOP
U17	54-53	4	IC,OP AMP,TLO72
U18	54-53		IC,OP AMP,TLO72
U19	54-132	2	IC,OP AMP,TL074CN3
U20	54-20	1	IC,ANALOG SWITCH,13201
U21	54-74LS04	1	IC,TTL,74LS04,HEX,INVERTERS
U22	54-53		IC,OP AMP,TLO72
U23	54-MC3302P	2	IC,COMPARATOR,LM3302
U24	54-MC3302P		IC,COMPARATOR,LM3302
U25	54-129	2	IC,D/A,AD7524,8BITS
U26	54-129		IC,D/A,AD7524,8BITS
U27	54-132		IC,OP AMP,TL074CN3
U28	54-53		IC,OP AMP,TLO72
VR1	54-451	1	IC,VOLTAGE REGULATOR,78LO5,5V
VR2	54-618	2	IC,VOLTAGE REG,78L12,+12V,35V
VR3	54-617	2	IC,VOLTAGE REG,79L12,-12V
VR4	54-618		IC,VOLTAGE REG,78L12,+12V,35V
VR5	54-617		IC,VOLTAGE REG,79L12,-12V

Table 5-5. A3 Signal Channel Interface (1 of 3)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	250-42	15	CAPACITOR,FXD,TANT,10µF,10%
C2			NOT ASSIGNED
C3	250-42		CAPACITOR,FXD,TANT,10µF,10%
C4			NOT ASSIGNED
C5			NOT ASSIGNED
C6	20-42		CAPACITOR,FXD,TANT,10µF,10%
C7	250-42		CAPACITOR,FXD,TANT,10µF,10%
C8	250-42		CAPACITOR,FXD,TANT,10µF,10%
C9	250-42		CAPACITOR,FXD,TANT,10µF,10%
C11	250-42		CAPACITOR,FXD,TANT,10µF,10%
C12	230-37	24	CAPACITOR,FXD,CER,0.1µF,20%
C13	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C14	250-163	2	CAPACITOR,FXD,ALUM POLAR
C15	250-163		CAPACITOR,FXD,ALUM POLAR
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	250-42		CAPACITOR,FXD,TANT,10µF,10%
C18	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C19	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C20	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C21	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C22	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C23	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C24	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C25	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C26	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C27	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C28	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C29	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C30	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C31	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C32	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C33			NOT ASSIGNED
C34	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C35	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C36	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C37	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C38	250-42		CAPACITOR,FXD,TANT,10µF,10%
C39	250-42		CAPACITOR,FXD,TANT,10µF,10%
C40	250-42		CAPACITOR,FXD,TANT,10µF,10%
C41	250-42		CAPACITOR,FXD,TANT,10µF,10%
C42	250-42		CAPACITOR,FXD,TANT,10µF,10%
C43	250-42		CAPACITOR,FXD,TANT,10µF,10%
C44	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C45	230-37		CAPACITOR,FXD,CER,0.1µF,20%
CR1	10-1N752A	1	DIODE,ZENER,1N752A,5.6V,5%
CR2	10-60	2	DIODE,RECTIFIER,IN4148,75V
CR3	10-60		DIODE,RECTIFIER,IN4148,75V
J1	551-577	1	CONNECTOR,SOCKET
L1	310-116	3	INDUCTOR,FXD,1.9µH
L2	310-116		INDUCTOR,FXD,1.9µH
L3	310-116		INDUCTOR,FXD,1.9µH
P1	552-5	1	CONNECTOR,ERO,PLUG,64/2R
P2	551-569	1	CONNECTOR,HEADER,1 ROW
R1	113-20K-.1	4	RESISTOR,FXD,MF,20K,.1%,0.25W
R2	113-20K-.1		RESISTOR,FXD,MF,20K,.1%,0.25W
R3	113-20K-.1		RESISTOR,FXD,MF,20K,.1%,0.25W
R4	113-20K-.1		RESISTOR,FXD,MF,20K,.1%,0.25W
R5	110-100-1	7	RESISTOR,FXD,MF,100,1%,0.25W
R6	110-1K-1	19	RESISTOR,FXD,MF,1K,1%,0.25W
R7	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W

Table 5-5. A3 Signal Channel Interface (2 of 3)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R8	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R9	110-10K-1	2	RESISTOR,FXD,MF,10K,1%,0.25W
R10	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R11	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R12	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R13	110-619-1	1	RESISTOR,FXD,MF,619,1%,0.25W
R14	110-11K-1	1	RESISTOR,FXD,MF,11K,1%,0.25W
R15	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R16	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R17	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R18	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R19	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R20	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R21	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R22	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R23	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R24	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R25	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R26	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R27	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R28	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R29	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R30	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R31	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R32	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R33	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R34	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
RN1	123-1K	1	RESISTOR,NETWORK,1K
TP1	702-17	17	TERMINAL,EYELET
TP2	702-17		TERMINAL,EYELET
TP3	702-17		TERMINAL,EYELET
TP4	702-17		TERMINAL,EYELET
TP5	702-17		TERMINAL,EYELET
TP6	702-17		TERMINAL,EYELET
TP7	702-17		TERMINAL,EYELET
TP8	702-17		TERMINAL,EYELET
TP9	702-17		TERMINAL,EYELET
TP10	702-17		TERMINAL,EYELET
TP11	702-17		TERMINAL,EYELET
TP12	702-17		TERMINAL,EYELET
TP13	702-17		TERMINAL,EYELET
TP14	702-17		TERMINAL,EYELET
TP15	702-17		TERMINAL,EYELET
TP16	702-17		TERMINAL,EYELET
TP17	702-17		TERMINAL,EYELET
U1	54-208	2	IC,ANALOG SWITCH,DG211
U2	54-208		IC,ANALOG SWITCH,DG211
U3	54-595	2	IC,OP-AMP,OP-27GP
U4	54-595		IC,OP-AMP,OP-27GP
U5	54-600	1	IC,TTL,74LS11,TRIPLE,AND
U6	54-453	1	IC,A/D,574,12 BIT,BINARY,25uS
U7	54-143	4	IC,TTL,74LS244,OCTAL,BUFFER
U8	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U9	54-74LS138	2	IC,TTL,74LS138,3 TO 8 DECODER
U10	54-74LS138		IC,TTL,74LS138,3 TO 8 DECODER
U11	54-41	2	IC,TTL,74LS374,OCTAL,D FLIP FLOP
U12	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U13	54-74LS08	1	IC,TTL,74LS08,QUAD,2 INPUT AND
U14	54-74LS04	1	IC,TTL,74LS04,HEX,INVERTERS
U15	54-74LS32	2	IC,TTL,74LS32,QUAD,2 INPUT OR

Table 5-5. A3 Signal Channel Interface (3 of 3)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
U16	54-74LS32		IC,TTL,74LS32,QUAD,2 INPUT OR
U17	54-41		IC,TTL,74LS374,OCTAL,D FLIP FLOP
U18	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U19	54-44	4	IC,TTL,74LS74,DUAL,D FLIP FLOP
U20	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U21	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U22	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
VR1	54-451	2	IC,VOLTAGE REGULATOR,78LO5
VR2	54-451		IC,VOLTAGE REGULATOR,78LO5

Table 5-6. A4 Sweeper Interface (1 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	250-42	3	CAPACITOR,FXD,TANT,10µF,10%
C2			NOT ASSIGNED
C3	220-820	1	CAPACITOR,FXD,MICA,820PF,5%
C4	210-20	1	CAPACITOR,FXD,PEST,0.01µF,10%
C5			NOT ASSIGNED
C6	230-11	3	CAPACITOR,FXD,CER,0.01µF,+80/-20%
C7	230-37	33	CAPACITOR,FXD,CER,0.1µF,20%
C8	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C9			NOT ASSIGNED
C10	223-10	2	CAPACITOR,FXD,MICA,10PF,5%
C11	223-10		CAPACITOR,FXD,MICA,10PF,5%
C12	230-11		CAPACITOR,FXD,CER,0.01µF,+80/-20%
C13	230-11		CAPACITOR,FXD,CER,0.01µF,+80/-20%
C14	220-33	1	CAPACITOR,FXD,MICA,33PF,5%
C15	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	250-58A	2	CAPACITOR,FXD,TANT,68µF,10%,6V
C18	250-42		CAPACITOR,FXD,TANT,10µF,10%
C19	250-42		CAPACITOR,FXD,TANT,10µF,10%
C20	250-58A		CAPACITOR,FXD,TANT,68µF,10%,6V
C21	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C22	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C23	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C24	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C25	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C26	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C27	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C28	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C29	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C30	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C31	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C32	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C33	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C34	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C35	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C36	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C37	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C38	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C39			NOT ASSIGNED
C40	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C41	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C42	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C43	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C44			NOT ASSIGNED
C45			NOT ASSIGNED
C46			NOT ASSIGNED
C47			NOT ASSIGNED
C48	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C49	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C50	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C51	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C52	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C53	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C54	230-37		CAPACITOR,FXD,CER,0.1µF,20%
CR1	54-604	1	IC,VOLTAGE REG,LM336B
CR2	10-1N758A	6	DIODE,ZENER,1N758A,10V,5%
CR3	10-1N758A		DIODE,ZENER,1N758A,10V,5%
CR4	10-1N751A	2	DIODE,ZENER,1N751A,5.1V,5%
CR5	10-1N751A		DIODE,ZENER,1N751A,5.1V,5%
CR6	10-60	11	DIODE,RECTIFIER,IN4148,75V

Table 5-6. A4 Sweeper Interface (2 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
CR7	10-60		DIODE,RECTIFIER,IN4148,75V
CR8	10-60		DIODE,RECTIFIER,IN4148,75V
CR9	10-11	1	DIODE,ZENER,1N750A,4.7V,5%
CR10	10-1N758A		DIODE,ZENER,1N758A,10V,5%
CR11	10-1N758A		DIODE,ZENER,1N758A,10V,5%
CR12	10-60		DIODE,RECTIFIER,IN4148,75V
CR13	10-60		DIODE,RECTIFIER,IN4148,75V
CR14	10-1N758A		DIODE,ZENER,1N758A,10V,5%
CR15	10-1N758A		DIODE,ZENER,1N758A,10V,5%
CR16	10-60		DIODE,RECTIFIER,IN4148,75V
CR17	10-60		DIODE,RECTIFIER,IN4148,75V
CR18	10-60		DIODE,RECTIFIER,IN4148,75V
CR19	10-60		DIODE,RECTIFIER,IN4148,75V
CR20	10-60		DIODE,RECTIFIER,IN4148,75V
CR21	10-60		DIODE,RECTIFIER,IN4148,75V
J1	551-577	1	CONNECTOR,SOCKET
L1	310-116	3	INDUCTOR,FXD,1.9µH
L2	310-116		INDUCTOR,FXD,1.9µH
L3	310-116		INDUCTOR,FXD,1.9µH
P1	552-5	1	CONNECTOR,PLUG
P2	551-569	1	CONNECTOR,HEADER
R1	110-5.11K-1	3	RESISTOR,FXD,MF,5.11K,1%,0.25W
R2	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R3	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R4	110-27.4K-1	1	RESISTOR,FXD,MF,27.4K,1%,0.25W
R5	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R6	101-1M-5	1	RESISTOR,FXD,CC,1M,5%,0.25W
R7	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R8	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R9	110-20.5K-1	1	RESISTOR,FXD,MF,20.5K,1%,0.25W
R10	156-5K-A	1	RESISTOR,TRIM,CER,5K
R11	110-17.8K-1	1	RESISTOR,FXD,MF,17.8K,1%,0.25W
R12	110-1.78K-1	1	RESISTOR,FXD,MF,1.78K,1%,0.25W
R13	110-46.4K-1	1	RESISTOR,FXD,MF,46.4K,1%,0.25W
R14	110-10K-1	31	RESISTOR,FXD,MF,10K,1%,0.25W
R15	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R16	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R17	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R18	101-10M-5	1	RESISTOR,FXD,CC,10M,5%,0.25W
R19	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R20	110-93.1K-1	5	RESISTOR,FXD,MF,93.1K,1%,0.25W
R21	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R22	110-511K-1	1	RESISTOR,FXD,MF,511K,1%,0.25W
R23	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R24	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R25	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R26	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R27	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R28	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R29	110-14.7K-1	2	RESISTOR,FXD,MF,14.7K,1%,0.25W
R30	110-5.11K-1		RESISTOR,FXD,MF,5.11K,1%,0.25W
R31	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R32	110-11K-1	1	RESISTOR,FXD,MF,11K,1%,0.25W
R33	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R34	110-215K-1	1	RESISTOR,FXD,MF,215K,1%,0.25W
R35	110-68.1K-1	2	RESISTOR,FXD,MF,68.1K,1%,0.25W
R36	110-28.7K-1	2	RESISTOR,FXD,MF,28.7K,1%,0.25W
R37	110-3.32K-1	6	RESISTOR,FXD,MF,3.32K,1%,0.25W
R38	101-3.3M-5	3	RESISTOR,FXD,CC,3.3M,5%,0.25W
R39	110-4.02K-1	1	RESISTOR,FXD,MF,4.02K,1%,0.25W

Table 5-6. A4 Sweeper Interface (3 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R40	110-14.7K-1		RESISTOR,FXD,MF,14.7K,1%,0.25W
R41	110-61.9K-1	1	RESISTOR,FXD,MF,61.9K,1%,0.25W
R42	110-33.2K-1	1	RESISTOR,FXD,MF,33.2K,1%,0.25W
R43	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R44	101-3.3M-5		RESISTOR,FXD,CC,3.3M,5%,0.25W
R45	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R46	110-93.1K-1		RESISTOR,FXD,MF,93.1K,1%,0.25W
R47	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R48	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R49	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R50	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R51	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R52	110-51.1K-1	2	RESISTOR,FXD,MF,51.1K,1%,0.25W
R53	110-51.1K-1		RESISTOR,FXD,MF,51.1K,1%,0.25W
R54	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R55	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R56	110-93.1K-1		RESISTOR,FXD,MF,93.1K,1%,0.25W
R57	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R58	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R59	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R60	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R61	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R62	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R63	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R64	110-93.1K-1		RESISTOR,FXD,MF,93.1K,1%,0.25W
R65	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R66	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R67	110-93.1K-1		RESISTOR,FXD,MF,93.1K,1%,0.25W
R68	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R69	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R70	110-100-1	3	RESISTOR,FXD,MF,100,1%,0.25W
R71	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R72	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R73	110-100K-1	2	RESISTOR,FXD,MF,100K,1%,0.25W
R74	101-3.3M-5		RESISTOR,FXD,CC,3.3M,5%,0.25W
R75	110-68.1K-1		RESISTOR,FXD,MF,68.1K,1%,0.25W
R76	110-28.7K-1		RESISTOR,FXD,MF,28.7K,1%,0.25W
R77	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R78	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R79	110-5.11K-1		RESISTOR,FXD,MF,5.11K,1%,0.25W
R80	110-24.9K-1	1	RESISTOR,FXD,MF,24.9K,1%,0.25W
TP1	702-17	22	TERMINAL,EYELET
TP2	702-17		TERMINAL,EYELET
TP3	702-17		TERMINAL,EYELET
TP4	702-17		TERMINAL,EYELET
TP5	702-17		TERMINAL,EYELET
TP6	702-17		TERMINAL,EYELET
TP7	702-17		TERMINAL,EYELET
TP8	702-17		TERMINAL,EYELET
TP9	702-17		TERMINAL,EYELET
TP10	702-17		TERMINAL,EYELET
TP11	702-17		TERMINAL,EYELET
TP12	702-17		TERMINAL,EYELET
TP13	702-17		TERMINAL,EYELET
TP14	702-17		TERMINAL,EYELET
TP15	702-17		TERMINAL,EYELET
TP16	702-17		TERMINAL,EYELET
TP17	702-17		TERMINAL,EYELET
TP18	702-17		TERMINAL,EYELET
TP19	702-17		TERMINAL,EYELET

Table 5-6. A4 Sweeper Interface (4 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
TP20	702-17		TERMINAL,EYELET
TP21	702-17		TERMINAL,EYELET
TP22	702-17		TERMINAL,EYELET
U1	50-9	2	IC,OP AMP,LF356
U2	54-53	2	IC,OP AMP,TLO72
U3	54-204	1	IC,OP AMP,LF398
U4	54-605	1	IC,VOLTAGE COMPARATOR
U5	54-132	2	IC,OP AMP,TL074CN3
U6	50-9		IC,OP AMP,LF356
U7	54-MC3302P	2	IC,COMPARATOR,LM3302
U8	54-53		IC,OP AMP,TLO72
U9	54-132		IC,OP AMP,TL074CN3
U10	54-MC3302P		IC,COMPARATOR,LM3302
U11	54-74LS132	2	IC,TTL,74LS132,QUAD,NAND SCHMITT
U12	54-74LS132		IC,TTL,74LS132,QUAD,NAND SCHMITT
U13	54-74LS04	1	IC,TTL,74LS04,HEX,INVERTERS
U14	54-96	1	1C,TTL,74LS09,QUAD,2 INPUT AND
U15	54-74LS32	1	IC,TTL,74LS32,QUAD,2 INPUT OR
U16	54-44	2	IC,TTL,74LS74,DUAL,D FLIP FLOP
U17	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U18	54-74LS138	2	IC,TTL,74LS138,3 TO 8 DECODER
U19	54-74LS138		IC,TTL,74LS138,3 TO 8 DECODER
U20	54-41	1	IC,TTL,74LS374,OCTAL,D FLIP FLOP
U21	54-103	1	1C,TTL,74LS373,OCTAL,TRANSPARENT
U22	54-74LS175	1	IC,TTL,74LS175,QUAD,D FLIP FLOP
U23	54-432	1	IC,D/A,AD7545,12 BIT,BINARY
U24	54-595	1	IC,OP-AMP,OP-27GP
U25	54-125	1	IC,TTL,74LS86,QUAD,2 INPUT XOR
U26	54-74LS00	1	IC,TTL,74LS00,QUAD,2 INPUT NAND

Table 5-7. A5 CPU (1 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
BT1	633-8	1	BATTERY,NICAD,2.4V
C1	250-58A	1	CAPACITOR,FXD,TANT,68µF,10%,6V
C2	230-35	1	CAPACITOR,FXD,CER,0.05µF,+85/-20%
C3			NOT ASSIGNED
C4	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C5	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C6	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C7	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C8	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C9	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C10	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C11	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C12	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C13	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C14	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C15	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C16	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C17	250-57	1	CAPACITOR,FXD,TANT,150µF,10%
C18	250-42	2	CAPACITOR,FXD,TANT,10µF,10%
C19	230-37	23	CAPACITOR,FXD,CER,0.1µF,20%
C20			NOT ASSIGNED
C21			NOT ASSIGNED
C22			NOT ASSIGNED
C23			NOT ASSIGNED
C24			NOT ASSIGNED
C25	250-42		CAPACITOR,FXD,TANT,10µF,10%
C26			NOT ASSIGNED
C27	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C28			NOT ASSIGNED
C29			NOT ASSIGNED
C30	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C31	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C32	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C33	230-37		CAPACITOR,FXD,CER,0.1µF,20%
CR1	10-60	3	DIODE,RECTIFIER,IN4148,75V
CR2	10-60		DIODE,RECTIFIER,IN4148,75V
CR3	10-60		DIODE,RECTIFIER,IN4148,75V
CR4	10-SI2	1	DIODE,RECTIFIER,IN4003,200V
J1			NOT ASSIGNED
J2	551-577	1	CONNECTOR,SOCKET
L1	310-116	1	INDUCTOR,FXD,1.9µH
P1	552-5	1	CONNECTOR,ERO,PLUG
P2	551-569	1	CONNECTOR,HEADER
Q1	20-24	4	TRANSISTOR,PNP,MJE371,SI
Q2	20-24		TRANSISTOR,PNP,MJE371,SI
Q3	20-24		TRANSISTOR,PNP,MJE371,SI
Q4	20-24		TRANSISTOR,PNP,MJE371,SI
R1	110-100K-1	2	RESISTOR,FXD,MF,100K,1%,0.25W
R2	110-22.6K-1	2	RESISTOR,FXD,MF,22.6K,1%,0.25W
R3	110-22.6K-1		RESISTOR,FXD,MF,22.6K,1%,0.25W
R4	110-1K-1	1	RESISTOR,FXD,MF,1K,1%,0.25W
R5	110-12.1K-1	1	RESISTOR,FXD,MF,12.1K,1%,0.25W
R6	110-46.4K-1	1	RESISTOR,FXD,MF,46.4K,1%,0.25W
R7	110-147-1	1	RESISTOR,FXD,MF,147,1%,0.25W
R8	110-10K-1	1	RESISTOR,FXD,MF,10K,1%,0.25W
R9	101-8.2M-5	1	RESISTOR,FXD,CC,8.2M,5%,0.25W
R10	156-100K-A	1	RESISTOR,TRIM,CER,100K
R11	110-196K-1	1	RESISTOR,FXD,MF,196K,1%,0.25W
R12	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R13	101-5.1M-5	1	RESISTOR,FXD,CC,5.1M,5%,0.25WW

Table 5-7. A5 CPU (2 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R14	110-511K-1	1	RESISTOR,FXD,MF,511K,1%,0.25W
R15	110-1M-1	4	RESISTOR,FXD,MF,1M,1%,0.25W
R16	110-422-1	1	RESISTOR,FXD,MF,422,1%,0.25W
R17	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R18	101-1M-1		RESISTOR,FXD,MF,1M,1%,0.25W
R19	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R20			NOT ASSIGNED
R21	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R22	110-511K-1		RESISTOR,FXD,MF,511K,1%,0.25W
R23	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R24	110-511-1	2	RESISTOR,FXD,MF,511,1%,0.25W
R25	110-511-1		RESISTOR,FXD,MF,511,1%,0.25W
R26	110-1M-1		RESISTOR,FXD,MF,1M,1%,0.25W
R27	110-1M-1		RESISTOR,FXD,MF,1M,1%,0.25W
R28	110-1M-1		RESISTOR,FXD,MF,1M,1%,0.25W
RN1	123-1K	1	RESISTOR,NETWORK,1K
TP1	702-17	7	TERM,EYELET
TP2	702-17		TERM,EYELET
TP3	702-17		TERM,EYELET
TP4	702-17		TERM,EYELET
TP5	702-17		TERM,EYELET
TP6	702-17		TERM,EYELET
TP7	702-17		TERM,EYELET
U1	54-320	1	IC,MICROPROCESSOR,8088-2
U2	54-317	1	IC,MICROPROCESSOR,8284A
U3	54-74LS73	1	IC,TTL,74LS73,DUAL,JK FLIP FLOP
U4	54-103	2	1C,TTL,74LS373,OCTAL,TRANSPARENT
U5	54-103		1C,TTL,74LS373,OCTAL,TRANSPARENT
U6	54-74LS08	1	IC,TTL,74LS08,QUAD,2 INPUT AND
U7	54-74LS138	2	IC,TTL,74LS138,3 TO 8 DECODER
U8	54-143	4	IC,TTL,74LS244,OCTAL,BUFFER
U9	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U10	54-344	2	IC,TTL,74LS245,OCTAL BIDIREC
U11	54-74LS138		IC,TTL,74LS138,3 TO 8 DECODER
U12	54-354	1	IC,TTL,74LS148,SINGLE,8 TO 3
U13	54-74LS00	1	IC,TTL,74LS00,QUAD,2 INPUT NAND
U14	54-74LS32	1	IC,TTL,74LS32,QUAD,2 INPUT OR
U15	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U16	54-44	1	IC,TTL,74LS74,DUAL,D FLIP FLOP
U17		5	EPROM,CALL FACTORY
U18			EPROM,CALL FACTORY
U19			EPROM,CALL FACTORY
U20			EPROM,CALL FACTORY
U21			EPROM,CALL FACTORY
U22	54-608	3	IC,MEMORY,43256C-L,SRAM,32K/8
U23	54-608		IC,MEMORY,43256C-L,SRAM,32K/8
U24	54-608		IC,MEMORY,43256C-L,SRAM,32K/8
U25	54-606	1	IC VOLTAGE COMPARATOR
U26	54-607	1	IC,CMOS,74HC32,QUAD,0R GATE
U27	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U28	54-344		IC,TTL,74LS245,OCTAL BIDIRECTIONAL
Y1	630-37	1	CRYSTAL,24MHz,.002%

Table 5-8. A6 Text & Graphics (1 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	230-37	27	CAPACITOR,FXD,CER,0.1µF,20%
C2	250-57	1	CAPACITOR,FXD,TANT,150µF,10%
C3	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C4	250-42	1	CAPACITOR,FXD,TANT,10µF,10%
C5	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C6	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C7	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C8	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C9	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C10	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C11	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C12	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C13	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C14	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C15	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C18	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C19	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C20	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C21	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C22	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C23	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C24	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C25	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C26	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C27	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C28	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C29	230-1	1	CAPACITOR,FXD,CER,4700PF,20%
C30	230-37		CAPACITOR,FXD,CER,0.1µF,20%
CR1	10-60	1	DIODE,RECTIFIER,IN4148,75V
L1	310-116	1	INDUCTOR,FXD,1.9µH
P1	552-5	1	CONNECTOR,ERO,PLUG
R1	110-100K-1	1	RESISTOR,FXD,MF,100K,1%,0.25W
R2	110-511-1	3	RESISTOR,FXD,MF,511,1%,0.25W
R3	110-511-1		RESISTOR,FXD,MF,511,1%,0.25W
R4	110-1K-1	4	RESISTOR,FXD,MF,1K,1%,0.25W
R5	110-10K-1	3	RESISTOR,FXD,MF,10K,1%,0.25W
R6	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R7	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R8	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R9	110-511-1		RESISTOR,FXD,MF,511,1%,0.25W
R10	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R11	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
TP1	702-17	10	TERMINAL,EYELET
TP2	702-17		TERMINAL,EYELET
TP3	702-17		TERMINAL,EYELET
TP4	702-17		TERMINAL,EYELET
TP5	702-17		TERMINAL,EYELET
TP6	702-17		TERMINAL,EYELET
TP7	702-17		TERMINAL,EYELET
TP8	702-17		TERMINAL,EYELET
TP9	702-17		TERMINAL,EYELET
TP10	702-17		TERMINAL,EYELET
U1	54-320	1	IC,MICROPROCESSOR,8088-2
U2		2	EPROM,CALL FACTORY
U3			EPROM,CALL FACTORY
U4	54-608	2	IC,MEMORY,43256C-L,SRAM,32K/8
U5	54-608		IC,MEMORY,43256C-L,SRAM,32K/8
U6	54-317	1	IC,MICROPROCESSOR,8284A

Table 5-8. A6 Text & Graphics (2 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
U7	54-103	2	1C,TTL,74LS373,OCTAL,TRANSPARENT
U8	54-74LS139	2	IC,TTL,74LS139,DUAL,2 TO 4 DEC
U9	54-74LS32	1	IC,TTL,74LS32,QUAD,2 INPUT OR
U10	54-74LS00	1	IC,TTL,74LS00,QUAD,2 INPUT NAND
U11	54-74LS367	2	IC,TTL,74LS367,HEX,BUS DRIVERS
U12	54-74LS08	2	IC,TTL,74LS08,QUAD,2 INPUT AND
U13	54-41	3	IC,TTL,74LS374,OCTAL,D FLIP FLOP
U14	54-41		IC,TTL,74LS374,OCTAL,D FLIP FLOP
U15	54-44	4	IC,TTL,74LS74,DUAL,D FLIP FLOP
U16	54-74LS139		IC,TTL,74LS139,DUAL,2 TO 4 DEC
U17	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U18	54-74LS138	1	IC,TTL,74LS138,3 TO 8 DECODER
U19	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U20	54-41		IC,TTL,74LS374,OCTAL,D FLIP FLOP
U21	54-143	2	IC,TTL,74LS244,OCTAL,BUFFER
U22	54-74LS08		IC,TTL,74LS08,QUAD,2 INPUT AND
U23	54-103		1C,TTL,74LS373,OCTAL,TRANSPARENT
U24	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U25	54-143		IC,TTL,74LS244,OCTAL,BUFFER
U26	54-74LS367		IC,TTL,74LS367,HEX,BUS DRIVERS
Y1	630-37	1	CRYSTAL,24MHz,.002%

Table 5-9. A7 Video Display Processor (1 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	223-82	1	CAPACITOR,FXD,MICA,82PF,5%
C2	250-19A	3	CAPACITOR,FXD,TANT,1µF,10%,35V
C3	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C4	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C5	230-37	52	CAPACITOR,FXD,CER,0.1µF,20%
C6	223-150	1	CAPACITOR,FXD,MICA,150PF,5%
C7	220-390	1	CAPACITOR,FXD,MICA,390PF,5%
C8	250-42	2	CAPACITOR,FXD,TANT,10µF,10%
C9	250-42		CAPACITOR,FXD,TANT,10µF,10%
C10			NOT ASSIGNED
C11			NOT ASSIGNED
C12	220-820	1	CAPACITOR,FXD,MICA,820PF,5%
C13	250-163	2	CAPACITOR,FXD,ALUM POLAR
C14	250-57	1	CAPACITOR,FXD,TANT,150µF,10%
C15	250-163		CAPACITOR,FXD,ALUM POLAR
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C18	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C19	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C20	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C21	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C22	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C23	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C24	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C25	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C26	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C27	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C28	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C29	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C30	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C31	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C32	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C33	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C34	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C35	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C36	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C37	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C38	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C39	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C40	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C41	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C42	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C43	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C44	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C45	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C46	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C47	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C48	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C49	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C50	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C51	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C52	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C53	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C54	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C55	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C56	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C57	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C58	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C59	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C60	230-37		CAPACITOR,FXD,CER,0.1µF,20%

Table 5-9. A7 Video Display Processor (2 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C61	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C62	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C63	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C64	223-110	1	CAPACITOR,FXD,MICA,110PF,5%
C65	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C66	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C67	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C68	230-11	1	CAPACITOR,FXD,CER,0.01µF,+80/-20%
CR1	10-60	5	DIODE,RECTIFIER,IN4148,75V
CR2	10-60		DIODE,RECTIFIER,IN4148,75V
CR3	10-60		DIODE,RECTIFIER,IN4148,75V
CR4	10-61	1	DIODE,VARACTOR,MVAM115,440pF
CR5	10-60		DIODE,RECTIFIER,IN4148,75V
CR6	10-60		DIODE,RECTIFIER,IN4148,75V
J1	551-577	4	CONNECTOR,SOCKET
J2	551-577		CONNECTOR,SOCKET
J3	551-577		CONNECTOR,SOCKET
J4	551-577		CONNECTOR,SOCKET
L1	310-116	3	INDUCTOR,FXD,1.9µH
L2	310-116		INDUCTOR,FXD,1.9µH
L3	310-116		INDUCTOR,FXD,1.9µH
L4	310-35	1	INDUCTOR,FXD,10µH
P1	552-5	1	CONNECTOR,ERO,PLUG
P2	551-569	4	CONNECTOR,HEADER
P3	551-569		CONNECTOR,HEADER
P4	551-569		CONNECTOR,HEADER
P5	551-569		CONNECTOR,HEADER
Q1	20-2N3563	2	TRANSISTOR,NPN,2N3563,SI
Q2	20-2N3563		TRANSISTOR,NPN,2N3563,SI
Q3	20-2N2218	2	TRANSISTOR,NPN,2N2218,SI
Q4	20-2N2218		TRANSISTOR,NPN,2N2218,SI
R1	110-1.5K-1	1	RESISTOR,FXD,MF,1.5K,1%,0.25W
R2	110-1K-1	13	RESISTOR,FXD,MF,1K,1%,0.25W
R3	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R4	110-22.1-1	14	RESISTOR,FXD,MF,22.1,1%,0.25W
R5	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R6	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R7	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R8	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R9	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R10	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R11	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R12	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R13	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R14	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R15	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R16	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R17	110-22.1-1		RESISTOR,FXD,MF,22.1,1%,0.25W
R18	110-2K-1	3	RESISTOR,FXD,MF,2K,1%,0.25W
R19	110-2K-1		RESISTOR,FXD,MF,2K,1%,0.25W
R20	110-100K-1	3	RESISTOR,FXD,MF,100K,1%,0.25W
R21	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R22	110-348K-1	1	RESISTOR,FXD,MF,348K,1%,0.25W
R23	110-10K-1	3	RESISTOR,FXD,MF,10K,1%,0.25W
R24	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R25	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R26	156-1K	1	RESISTOR,TRIM,CER,1K
R27	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R28	110-30.1K-1	1	RESISTOR,FXD,MF,30.1K,1%,0.25W
R29	110-110-1	2	RESISTOR,FXD,MF,110,1%,0.25W

Table 5-9. A7 Video Display Processor (3 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R30	110-750-1	3	RESISTOR,FXD,MF,750,1%,0.25W
R31	110-750-1		RESISTOR,FXD,MF,750,1%,0.25W
R32	110-750-1		RESISTOR,FXD,MF,750,1%,0.25W
R33	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R34	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R35	110-2K-1		RESISTOR,FXD,MF,2K,1%,0.25W
R36	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R37	110-205-1	1	RESISTOR,FXD,MF,205,1%,0.25W
R38	110-100-1	2	RESISTOR,FXD,MF,100,1%,0.25W
R39	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R40	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R41	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R42	110-100-1		RESISTOR,FXD,MF,100,1%,0.25W
R43	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R44	110-42.2-1	1	RESISTOR,FXD,MF,42.2,1%,0.25W
R45	110-61.9-1	1	RESISTOR,FXD,MF,61.9,1%,0.25W
R46	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R47	110-4.99K-1	1	RESISTOR,FXD,MF,4.99K,1%,0.25W
R48	156-50K	1	RESISTOR,TRIM,CER,50K
R49	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R50	110-110-1		RESISTOR,FXD,MF,110,1%,0.25W
R51	110-100K-1		RESISTOR,FXD,MF,100K,1%,0.25W
R52	110-5.11K-1	2	RESISTOR,FXD,MF,5.11K,1%,0.25W
R53	110-5.11K-1		RESISTOR,FXD,MF,5.11K,1%,0.25W
R54	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
U1	54-448	1	IC,MICROPROCESSOR,82720
U2	54-447	1	IC,TTL,74LS163
U3	54-122	1	IC,TTL,74LS194,4 BIT SHIFT REG
U4	54-350	1	IC,TTL,74LS273,OCTAL,D-TYPE
U5	54-446	2	IC,TTL,74LS257,QUAD,DATA SELECT
U6	54-446		IC,TTL,74LS257,QUAD,DATA SELECT
U7	54-44	5	IC,TTL,74LS74,DUAL,D FLIP FLOP
U8	54-74LS139	1	IC,TTL,74LS139,DUAL,2 TO 4 DEC
U9	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U10	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U11	54-74LS367	1	IC,TTL,74LS367,HEX,BUS DRIVERS
U12	54-74LS112	1	IC,TTL,74LS112,DUAL,JK FLIP FLOP
U13	50-9	1	IC,OP AMP,LF356
U14	54-74LS132	2	IC,TTL,74LS132,QUAD,NAND SCHMITT
U15	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U16	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U17	54-74LS122	1	IC,TTL,74LS122,SINGLE,MULTIVIBRATOR
U18	54-74LS266	1	IC,TTL,74LS266,QUAD,2 INPUT XNOR
U19	54-96	1	1C,TTL,74LS09,QUAD,2 INPUT AND
U20	54-74LS20	1	IC,TTL,74LS20,DUAL,4 INPUT NAND
U21	54-74LS00	1	IC,TTL,74LS00,QUAD,2 INPUT NAND
U22	54-74LS04	2	IC,TTL,74LS04,HEX,INVERTERS
U23	54-74LS04		IC,TTL,74LS04,HEX,INVERTERS
U24	54-74LS08	1	IC,TTL,74LS08,QUAD,2 INPUT AND
U25	54-378	12	IC,MEMORY,TMS4416
U26	54-378		IC,MEMORY,TMS4416
U27	54-378		IC,MEMORY,TMS4416
U28	54-378		IC,MEMORY,TMS4416
U29	54-378		IC,MEMORY,TMS4416
U30	54-378		IC,MEMORY,TMS4416
U31	54-378		IC,MEMORY,TMS4416
U32	54-378		IC,MEMORY,TMS4416
U33	54-378		IC,MEMORY,TMS4416
U34	54-378		IC,MEMORY,TMS4416
U35	54-378		IC,MEMORY,TMS4416

Table 5-9. A7 Video Display Processor (4 of 4)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
U36	54-378		IC,MEMORY,TMS4416
U37	54-611	6	IC,HCTCMOS,74HCT166
U38	54-610	6	IC,HCTCMOS,74HCT245,OCTAL,BUS
U39	54-611		IC,HCTCMOS,74HCT166
U40	54-610		IC,HCTCMOS,74HCT245,OCTAL,BUS
U41	54-611		IC,HCTCMOS,74HCT166
U42	54-610		IC,HCTCMOS,74HCT245,OCTAL,BUS
U43	54-611		IC,HCTCMOS,74HCT166
U44	54-610		IC,HCTCMOS,74HCT245,OCTAL,BUS
U45	54-611		IC,HCTCMOS,74HCT166
U46	54-610		IC,HCTCMOS,74HCT245,OCTAL,BUS
U47	54-611		IC,HCTCMOS,74HCT166
U48	54-610		IC,HCTCMOS,74HCT245,OCTAL,BUS
U49	54-74LS132		IC,TTL,74LS132,QUAD,NAND SCHMITT

Table 5-10. A8 System GPIB (1 of 1)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	250-57	1	CAPACITOR,FXD,TANT,150µF,10%
C2	230-37	10	CAPACITOR,FXD,CER,0.1µF,20%
C3	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C4	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C5	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C6	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C7	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C8	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C9	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C10	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C11	230-37		CAPACITOR,FXD,CER,0.1µF,20%
J1	551-741	1	CONNECTOR,SUBMIN
RN1	123-1K	1	RESISTOR,NETWORK,1K
S1	430-227	1	SWITCH.DIP,12 PIN,SLIDE
U1	54-454	1	IC,MICROPROCESSOR,8291A,GPIB
U2	54-443	4	IC,DIGITAL INTERFACE,MC3448
U3	54-443		IC,DIGITAL INTERFACE,MC3448
U4	54-443		IC,DIGITAL INTERFACE,MC3448
U5	54-443		IC,DIGITAL INTERFACE,MC3448
U6	54-74LS32	1	IC,TTL,74LS32,QUAD,2 INPUT OR
U7	54-74LS08	1	IC,TTL,74LS08,QUAD,2 INPUT AND
U8	54-74LS04	1	IC,TTL,74LS04,HEX
U9	54-74LS368	1	IC,TTL,74LS368,HEX

Table 5-11. A10 Dedicated GPIB (1 of 1)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	230-37	9	CAPACITOR,FXD,CER,0.1µF,20%
C2	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C3	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C4	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C5	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C6	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C7	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C8	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C9	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C10	250-58A	1	CAPACITOR,FXD,TANT,68µF,10%,6V
C11	250-42	1	CAPACITOR,FXD,TANT,10µF,10%
J1	551-741	1	CONNECTOR,SUBMIN
J2	551-577	1	CONNECTOR,SOCKET
P1			NOT ASSIGNED
P2	551-571	2	CONNECTOR,HEADER
P3	551-571		CONNECTOR,HEADER
R1	110-10K-1	2	RESISTOR,FXD,MF,10K,1%,0.25W
R2	110-20.5K-1	1	RESISTOR,FXD,MF,20.5K,1%,0.25W
R3	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
U1	54-601	1	IC,MICROPROCESSOR,TMS9914ANL
U2	54-602	1	IC,DIG INTERFACE,SN75160B
U3	54-603	1	IC,DIG INTERFACE,SN7561B
U4	54-344	1	IC,TTL,74LS245,OCTAL BIDIREC
U5	54-74LS132	2	IC,TTL,74LS132,QUAD,NAND SCHMITT
U6	54-74LS132		IC,TTL,74LS132,QUAD,NAND SCHMITT
U7	54-44	1	IC,TTL,74LS74,DUAL,D FLIP FLOP
U8	54-74LS138	1	IC,TTL,74LS138,3 TO 8 DECODER

Table 5-12. A9 Motherboard (1 of 1)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	230-32	2	CAPACITOR,FXD,CER,0.033µF,20%
C2	230-32		CAPACITOR,FXD,CER,0.033µF,20%
J1	552-4	7	CONNECTOR,VERTICAL
J2	552-4		CONNECTOR,VERTICAL
J3	552-4		CONNECTOR,VERTICAL
J4	552-4		CONNECTOR,VERTICAL
J5	552-4		CONNECTOR,VERTICAL
J6	552-4		CONNECTOR,VERTICAL
J7	552-4		CONNECTOR,VERTICAL
P1	551-570	2	CONNECTOR,HEADER
P2	551-533	2	CONNECTOR,HEADER
P3	551-567	1	CONNECTOR,HEADER
P4	551-709	1	CONNECTOR,HEADER
P5	551-533		CONNECTOR,HEADER
P6	551-566	1	CONNECTOR,HEADER
P7	551-743	1	CONNECTOR,HEADER
P8	551-570		CONNECTOR,HEADER
P9	551-534	2	CONNECTOR,HEADER
P10	551-534		CONNECTOR,HEADER
P11	551-750	1	CONNECTOR,HEADER

Table 5-13. A11 Switch Mounting (1 of 1)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
P1	551-567	1	CONNECTOR,HEADER
R1	146-7	1	RESISTOR,VARIABLE,CER,100
R2	110-100-1	1	RESISTOR,FXD,MF,100,1%,0.25W
S1	430-131	4	SWITCH,PUSH BUTTON,1STA
S2	430-131		SWITCH,PUSH BUTTON,1STA
S3	430-131		SWITCH,PUSH BUTTON,1STA
S4	430-131		SWITCH,PUSH BUTTON,1STA

Table 5-14. A12 Power Supply (1 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	250-160	2	CAP,FXD,ALUM,POLAR,3300MF
C2	230-37	9	CAPACITOR,FXD,CER,0.1µF,20%
C3	250-42	7	CAPACITOR,FXD,TANT,10µF,10%
C4	250-19A	7	CAPACITOR,FXD,TANT,1µF,10%,35V
C5	250-160		CAP,FXD,ALUM,POLAR,3300MF
C6	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C7	250-42		CAPACITOR,FXD,TANT,10µF,10%
C8	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C9	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C10	250-42		CAPACITOR,FXD,TANT,10µF,10%
C11	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C12	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C13	250-42		CAPACITOR,FXD,TANT,10µF,10%
C14	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C15	250-159	1	CAP,FXD,ALUM,POLAR,10000MF
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	250-42		CAPACITOR,FXD,TANT,10µF,10%
C18	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C19	250-138	1	CAP,FXD,ALUM,POLAR,33000µF
C20			NOT ASSIGNED
C21	250-42		CAPACITOR,FXD,TANT,10µF,10%
C22	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C23	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C24	250-42		CAPACITOR,FXD,TANT,10µF,10%
C25	250-19A		CAPACITOR,FXD,TANT,1µF,10%,35V
C26	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C27	210-28	3	CAPACITOR,FXD,PEST,0.047µF,10%
C28	210-28		CAPACITOR,FXD,PEST,0.047µF,10%
C29	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C30	210-28		CAPACITOR,FXD,PEST,0.047µF,10%
C31	230-37		CAPACITOR,FXD,CER,0.1µF,20%
CR1	10-67	2	DIODE,RECTIFIER,100V
CR2	10-67		DIODE,RECTIFIER,100V
CR3	10-77	1	DIODE,RECTIFIER,26MB5A,50V
CR4	10-SI2	15	DIODE,RECTIFIER,IN4003,200V
CR5	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR6	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR7	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR8	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR9	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR10	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR11	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR12	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR13	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR14	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR15	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR16	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR17	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR18	10-SI2		DIODE,RECTIFIER,IN4003,200V
CR19	15-32	1	INDICATOR,LED,YELLOW
P1	551-99	1	CONNECTOR,HDR,PCB MNT
P2	551-709	1	CONNECTOR,HEADER
Q1	20-2N3694	1	TRANSISTOR,NPN,2N3694,SI
R1	110-20.5K-1	2	RESISTOR,FXD,MF,20.5K,1%,0.25W
R2	110-2.61K-1	2	RESISTOR,FXD,MF,2.61K,1%,0.25W
R3	110-237-1	6	RESISTOR,FXD,MF,237,1%,0.25W
R4	110-20.5K-1		RESISTOR,FXD,MF,20.5K,1%,0.25W
R5	110-1.33K-1	2	RESISTOR,FXD,MF,1.33K,1%,0.25W
R6	110-121-1	2	RESISTOR,FXD,MF,121,1%,0.25W
R7	110-2.61K-1		RESISTOR,FXD,MF,2.61K,1%,0.25W

Table 5-14. A12 Power Supply (2 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R8	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R9	110-1.33K-1		RESISTOR,FXD,MF,1.33K,1%,0.25W
R10	110-121-1		RESISTOR,FXD,MF,121,1%,0.25W
R11	110-10K-1	3	RESISTOR,FXD,MF,10K,1%,0.25W
R12	110-2.05K-1	1	RESISTOR,FXD,MF,2.05K,1%,0.25W
R13	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R14	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R15	110-715-1	2	RESISTOR,FXD,MF,715,1%,0.25W
R16	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R17	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R18	110-715-1		RESISTOR,FXD,MF,715,1%,0.25W
R19	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R20	110-1K-1	3	RESISTOR,FXD,MF,1K,1%,0.25W
R21	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R22	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R23	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
RT1	35-9	2	THERMISTER,POSITIVE T.C.
RT2	35-9		THERMISTER,POSITIVE T.C.
RT3	35-13	1	THERMISTOR,POSITIVE
SW1	695-1	1	THERMOSTAT,TEMPERATURE SENSING
TP1			NOT ASSIGNED
TP2			NOT ASSIGNED
TP3	702-17	2	TERMINAL,EYELET
TP4	702-17		TERMINAL,EYELET
VR1	54-333	2	IC,VOLTAGE REGULATOR,LM317
VR2	54-619	2	IC,VOLTAGE REG,LM337T
VR3	54-333		IC,VOLTAGE REGULATOR,LM317
VR4	54-619		IC,VOLTAGE REG,LM337T
VR5	54-620	1	IC,VOLTAGE REG,LM350K
VR6	54-573	2	IC,VOLTAGE REGULATOR,LM338
VR7	54-573		IC,VOLTAGE REGULATOR,LM338

Table 5-15. A13 Front Panel (1 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
C1	230-37	13	CAPACITOR,FXD,CER,0.1µF,20%
C2	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C3	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C4			NOT ASSIGNED
C5	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C6	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C7	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C8	250-42	2	CAPACITOR,FXD,TANT,10µF,10%
C9	250-42		CAPACITOR,FXD,TANT,10µF,10%
C10	210-18	1	CAPACITOR,FXD,PEST,0.22µF,20%
C11	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C12	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C13	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C14	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C15	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C16	230-37		CAPACITOR,FXD,CER,0.1µF,20%
C17	230-37		CAPACITOR,FXD,CER,0.1µF,20%
CR1	10-60	5	DIODE,RECTIFIER,IN4148
CR2	10-60		DIODE,RECTIFIER,IN4148
CR3	10-60		DIODE,RECTIFIER,IN4148
CR4	10-60		DIODE,RECTIFIER,IN4148
CR5	10-60		DIODE,RECTIFIER,IN4148
CR6	15-32	10	INDICATOR,LED,YELLOW
CR7	15-32		INDICATOR,LED,YELLOW
CR8	15-32		INDICATOR,LED,YELLOW
CR9	15-32		INDICATOR,LED,YELLOW
CR10	15-32		INDICATOR,LED,YELLOW
CR11	15-32		INDICATOR,LED,YELLOW
CR12	15-32		INDICATOR,LED,YELLOW
CR13	15-31	2	INDICATOR,LED,RED
CR14	15-31		INDICATOR,LED,RED
CR15	15-32		INDICATOR,LED,YELLOW
CR16	15-32		INDICATOR,LED,YELLOW
CR17	15-32		INDICATOR,LED,YELLOW
L1	310-116	2	INDUCTOR,FXD,1.9µH
L2	310-116		INDUCTOR,FXD,1.9µH
P1	551-570	1	CONNECTOR,HEADER
P2	551-566	1	CONNECTOR,HEADER
Q1	20-17	1	TRANSISTOR,FET,J112,SI
Q2	20-2N4410	3	TRANSISTOR,NPN,SI
Q3	20-2N4410		TRANSISTOR,NPN,SI
Q4	20-2N4410		TRANSISTOR,NPN,SI
R1	110-1K-1	6	RESISTOR,FXD,MF,1K,1%,0.25W
R2	110-20.5K-1	2	RESISTOR,FXD,MF,20.5K,1%,0.25W
R3	110-20.5K-1		RESISTOR,FXD,MF,20.5K,1%,0.25W
R4	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R5	101-2.2M-5	1	RESISTOR,FXD,CC,2.2M,5%,0.25W
R6			NOT ASSIGNED
R7	110-187K-1	2	RESISTOR,FXD,MF,187K,1%,0.25W
R8	110-7.15K-1	2	RESISTOR,FXD,MF,7.15K,1%,0.25W
R9	110-10K-1	5	RESISTOR,FXD,MF,10K,1%,0.25W
R10	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R11	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R12	110-7.15K-1		RESISTOR,FXD,MF,7.15K,1%,0.25W
R13	110-187K-1		RESISTOR,FXD,MF,187K,1%,0.25W
R14	110-287K-1	1	RESISTOR,FXD,MF,287K,1%,0.25W
R15	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R16	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R17	110-10K-1		RESISTOR,FXD,MF,10K,1%,0.25W
R18	110-34.8K-1	1	RESISTOR,FXD,MF,34.8K,1%,0.25W

Table 5-15. A13 Front Panel (2 of 2)

REF DES	WILTRON PART NO.	QTY	DESCRIPTION
R19	110-6.81K-1	1	RESISTOR,FXD,MF,6.81K,1%,0.25W
R20	110-3.32K-1	3	RESISTOR,FXD,MF,3.32K,1%,0.25W
R21	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R22	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R23	110-5.62K-1	1	RESISTOR,FXD,MF,5.62K,1%,0.25W
R24	110-3.32K-1		RESISTOR,FXD,MF,3.32K,1%,0.25W
R25	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R26	110-1K-1		RESISTOR,FXD,MF,1K,1%,0.25W
R27	110-237-1	12	RESISTOR,FXD,MF,237,1%,0.25W
R28	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R29	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R30	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R31	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R32	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R33	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R34	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R35	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R36	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R37	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
R38	110-237-1		RESISTOR,FXD,MF,237,1%,0.25W
RN1	123-1K	2	RESISTOR,NETWORK,1K
RN2	123-1K		RESISTOR,NETWORK,1K
TP1	702-17	1	TERMINAL,EYELET
U1	54-595	1	IC,OP-AMP,OP-27GP
U2	54-53	1	IC,OP AMP,TLO72
U3	54-44	2	IC,TTL,74LS74,DUAL,D FLIP FLOP
U4	54-74LS138	1	IC,TTL,74LS138,3 TO 8 DECODER
U5	54-143	1	IC,TTL,74LS244,OCTAL,BUFFER
U6	54-44		IC,TTL,74LS74,DUAL,D FLIP FLOP
U7	54-41	2	IC,TTL,74LS374,OCTAL,D FLIP FLOP
U8	54-41		IC,TTL,74LS374,OCTAL,D FLIP FLOP
U9	54-354	2	IC,TTL,74LS148
U10	54-354		IC,TTL,74LS148

6A-1 OVERALL 561 CIRCUIT DESCRIPTION

The 561 is a Scalar Network Analyzer that uses state-of-the-art digital control and computational circuitry to enhance it's accuracy and repeatability. An overall block diagram is shown in Figure 6A-1.

An 8088 microprocessor with a sixteen bit internal bus and an eight bit external bus is the central processing unit (CPU) of the system. This CPU is located on the A5 PCB and communicates with all other subsystems through a main bus located on the motherboard of the instrument. Functions that the CPU monitors and controls include measurement (A1,A2, and A3), display (A7), printing (A6), sweeper interface (A4), plotting (A10), external control (A8), and the user interface (A13). Figure 6A-1 illustrates the interaction of these PCBs.

The interface to all of these PCBs is memory mapped. This means that each function that the 561 performs is at a specific address that the CPU either reads data from or writes data to. Each PCB may therefore have as many addresses mapped to it as are needed to communicate with the CPU.

The CPU is interrupt driven, meaning that when a particular subassembly must communicate with the CPU it generates an interrupt request (IRQ). The CPU then services each interrupt based on when it was generated and the level of priority assigned to that particular interrupt.

6A-1.1 The Measurement Process

One of the major differences between the Model 561 Scalar Network Analyzer and more conventional SNAs (such as the Model 560) is that it uses linear amplifiers instead of log amplifiers. The conversion to logarithmic form is performed digitally using look-up tables. This allows for more stable accurate measurements and easier calibration than more conventional oscilloscope-like SNAs.

A1PCB and A2PCB are identical PCBs that process different channels of measurement data. The A1 PCB processes the R1 and R2 channels and the A2 PCB processes the A and B channels. Since these two PCBs are functionally identical, they are interchangeable. These units consist of an Input Module, Amplifiers, Filters, Multiplexer, Nulling, Sample and Hold, Log Conformity and Temperature Compensation Circuits.

The Input Module uses switching Field Effect Transistors (FETs) to multiplex the two input channels and provide a high impedance measurement input. Additional FETs break the signal path and provide a short circuit to the input of the amplifier chain for purposes of autozeroing.

The output of the Input Module is passed to the Amplifier chain. The amplifier chain has a differential input instrumentation amplifier that provides common mode rejection and programmable gain. The gain ranges are: X1, X10, X100, and X1000. Three additional stages of amplification boost the voltage levels to the levels required.

Filtering is achieved using switched capacitor filters to smooth the signal. Variations in the levels of smoothing desired are achieved by switching in different values of capacitors.

Nulling circuitry nulls out any dc offsets produced in the amplification circuitry.

The Multiplexer switches in the necessary log conformity and temperature compensation voltages as well as the signal from the output of the amplification and filtering circuits.

The sample and hold circuitry samples the output of the multiplexer and is the final stage of the A1/A2 PCBs. This circuit provides the input to subsequent PCBs.

Compensation for temperature variation is achieved in software using the voltage produced by a thermistor in a voltage divider network. The log conformity is achieved using a software lookup table.

The A3 PCB is the signal channel interface. This circuit digitizes the signal from the A1/A2 PCBs. Additionally it provides control signals for the A1/A2 PCBs and provides the drive signals for the internal quiet data bus.

The A4 PCB is the sweeper interface circuitry. This PCB uses the analog voltages provided by the sweeper that were originally intended for conventional analog type SNAs. It then converts them to the necessary digital information required to interface to the CPU. It then provides the required dwell signals to the sweeper when making measurements at discrete frequency points thus driving the sweeper to output the signals requested by the CPU.

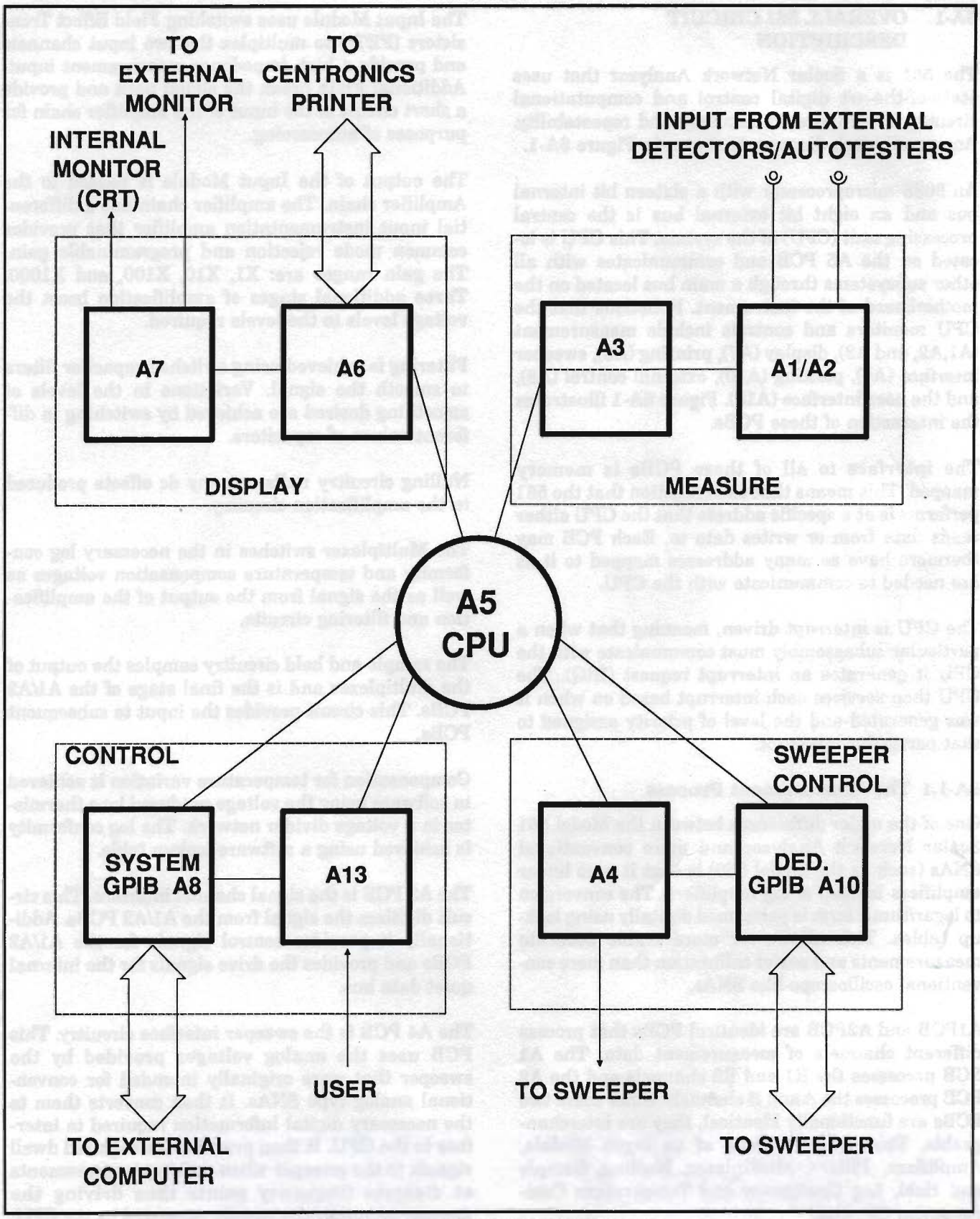

Figure 6A-1. 561 Overall Block Diagram

The A5 PCB is the CPU. It consists of a microprocessor, battery-backed nonvolatile RAM, I/O Ports decode logic and ROM-based operating system.

The Microprocessor controls the 561. As previously described, it interfaces to all major subcircuits and monitors and controls these circuits. The operating system is ROM-based and contains all of the primary functions of the 561. The Battery-backed RAM allows setup information to be retained even when powered down and disconnected from the line voltage. The decode circuitry decodes the addresses of the RAM, ROM, and I/O ports used to interface with the rest of the instrument. The I/O ports control the interface to the other subassemblies in the system.

The A6 PCB is the TGP (text and graphics display processor). This is a graphics subsystem that controls the display and printing capabilities of the 561. The CPU treats the TGP as an intelligent terminal and communicates with it through a combination of ASCII characters and escape sequences. It then sends high level commands to the A7 PCB Video Display Processor (VDP). All communications between the CPU and the VDP occur through the A6 PCB.

The hardcopy interface consists of a 50k byte buffer and a Centronics compatible hardware driver circuit. The hardcopy function is interrupt driven.

The A7 PCB is the video display processor. It provides all of the direct interface to the CRT assembly. This PCB receives high level commands from the A6 PCB. This PCB consists of a dedicated graphics display processor, memory, video driving circuitry, control and timing circuitry.

The A8 PCB is the interface to the 561 system General Purpose Interface Bus (GPIB). It has all necessary control circuitry required for the handshaking and data transfer through the GPIB bus.

6B-1 A1/A2 SIGNAL CHANNEL AMPLIFIER PCB FUNCTIONAL DESCRIPTION

The 561 Scalar Network Analyzer contains two identical and interchangeable signal channel amplifier circuit boards, designated A1 and A2. The board in the A1 slot of the card frame processes the R1 and R2 measurement channels and the board in the A2 slot processes the A and B channels.

Since the A1 and A2 circuit boards are functionally identical, only the operation of the A2 board will be considered here. If considering the A1 board, simply substitute channel R1 for all references to channel A and substitute channel R2 for all references to channel B. For a block diagram of the Input Module, refer to Figure 6B-1. Also refer to the A1/A2 block diagram (Figure 6B-2), the parts locator diagram (Figure 6B-3), and the schematic (Figure 6B-4) located on the fold-out pages.

Figure 6B-2 is a simplified functional block diagram of the A1/A2 PCB. As shown, this board contains an input switching module, a gain switchable amplifier chain, a smoothing filter, a five-way multiplexer, and a sample-and-hold amplifier. The first three functions are controlled by data that is routed from the CPU (A5) PCB via the quiet data bus and stored in latches. Signals from the Signal Channel Interface (A3) PCB directly control the five-way multiplexer and the sample-and-hold amplifier.

6B-1.1 Input Switching Module

Detected DC voltages in the region of 1 microvolt to 2 volts from detectors/autotesters are routed from the front panel A and B connectors to the two 5- pin plugs on the input switching module. Channel A is connected to P1 of the module, and channel B to P2.

The Input Switching Module contains switching field effect transistors (FETs) that multiplex the signal channel amplifier gain stages between the A and B inputs presented to the board. It also contains switching FETs to break the signal path from each detector/autotester and present a short circuit to the input of the amplifier chain for the purpose of autozeroing.The Input Switching Module provides no amplification. It provides switching functions only.

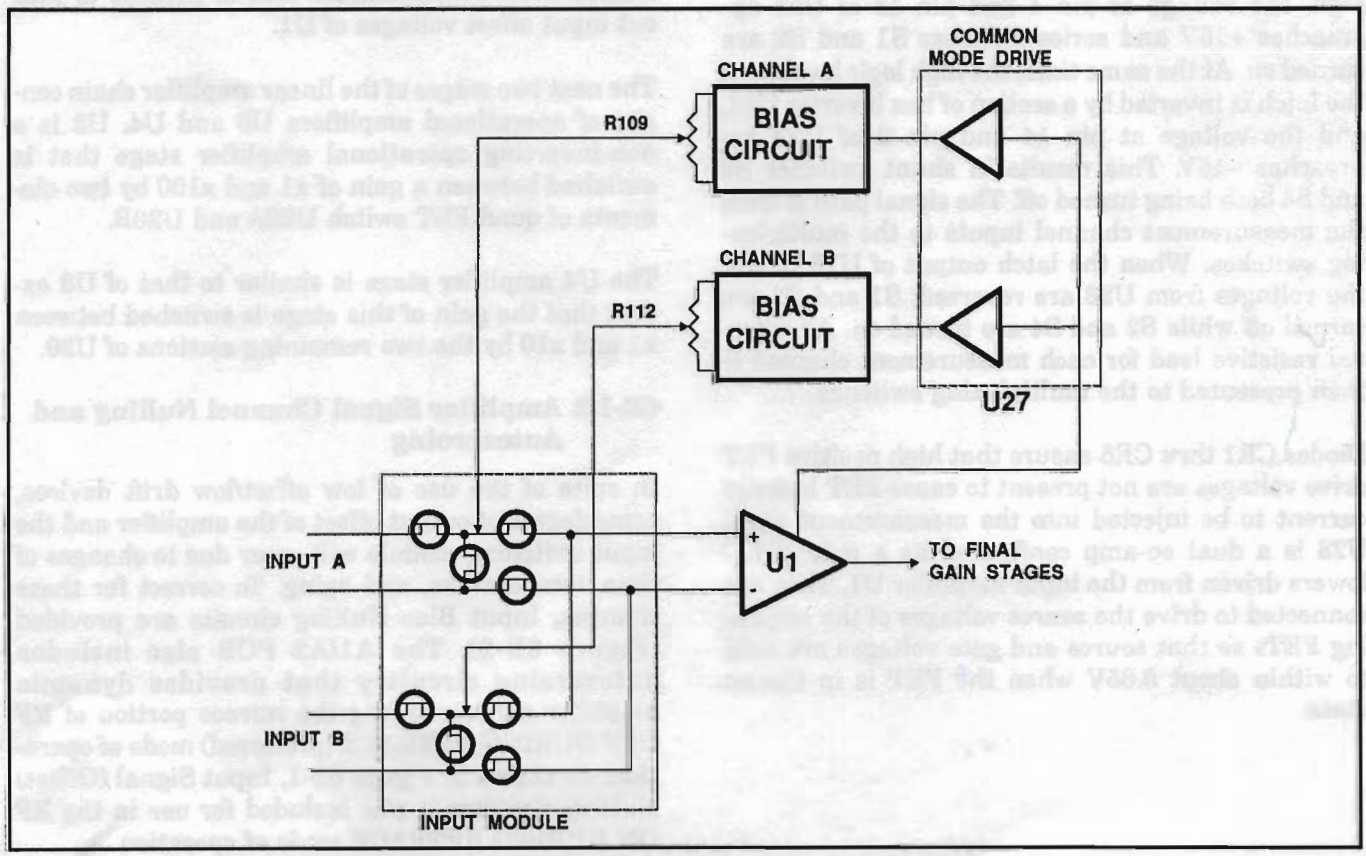

Figure 6B-1. Switching Arrangement of Input Module

Figure 6B-1 is a simplified representation of the switching arrangement of the Input Switching Module and the associated Input Bias Nulling feedback paths from the amplifier chain. This should serve as a general overview before referring to the schematic. A latched output of octal latch U15 is used to switch between A and B channels. When the latch output is high, the voltage at pin 1 and pin 13 of U24 approaches +15V and switches S5 and S6 are turned on. The high output of U15 is inverted by one section of the hex inverter U21C, causing the voltage at pin 2 and pin 14 of U24 to approach –15 V. This ensures that switches S7 and S8 are turned off (open); channel A is the measurement channel path that is routed through to the first stage of the amplifier chain. When the latched output of U15 is low, the opposite occurs; channel B is routed through to the amplifier.

Another latched output from hex latch integrated circuit U16 pin 15 is used to switch the external measuring device (detector/autotester) out of circuit and present a short circuit to the input of the amplifier chain. Since the measurement path is multiplexed after this point, the circuitry switches the two channels in parallel. When the latch output is high, the voltage at pin 1 and pin 13 of U23 approaches +15V and series switches S1 and S2 are turned on. At the same time, the high logic level from the latch is inverted by a section of hex inverter U21, and the voltage at pin 14 and pin 2 of U23 approaches –15V. This results in shunt switches S2 and S4 both being turned off. The signal path is from the measurement channel inputs to the multiplexing switches. When the latch output of U16 is low, the voltages from U23 are reversed; S1 and S3 are turned off while S2 and S4 are turned on. An internal resistive load for each measurement channel is then presented to the multiplexing switches.

Diodes CR1 thru CR8 ensure that high positive FET drive voltages are not present to cause FET leakage current to be injected into the measurement path. U28 is a dual op-amp configured as a pair of followers driven from the input amplifier U1. They are connected to drive the source voltages of the switching FETs so that source and gate voltages are held to within about 0.65V when the FET is in the on state.

6B-1.2 Amplifier Chain

The signal channel amplifier chain of the 561 Scalar Network Analyzer is a linear amplifier; there is no hardware log amplifier on the board. The necessary log conversion is done in the instrument's software. The software log conversion is done using a logarithmic look-up table over 10 dB of range (+2 dB for hysteresis), and then switching the gain of the signal channel amplifier in decade steps.

The multiplexed channel measurement signal from the Input Switching Module is applied to the differential inputs of the instrumentation amplifier U1. An instrumentation amplifier is used as the first stage of the linear amplifier chain because of its very high common mode rejection. This is necessary to extract the very small detected voltages from the high level of common mode interference that may be present on the input signals. U1 is a programmable gain amplifier that can be switched between four decade gains: x1, x10, x100, and x1000. The gains are switched by the dual four-channel multiplexer, U2 via latched outputs from U15.

Capacitors C1, C2, and C3 filter out high frequency interference. Potentiometer R40 is present to null out input offset voltages of U1.

The next two stages of the linear amplifier chain consist of operational amplifiers U3 and U4. U3 is a non-inverting operational amplifier stage that is switched between a gain of x1 and x100 by two elements of quad FET switch U20A and U20B.

The U4 amplifier stage is similar to that of U3 except that the gain of this stage is switched between x1 and x10 by the two remaining sections of U20.

6B-1.3 Amplifier Signal Channel Nulling and Autozeroing

In spite of the use of low offset/low drift devices, some degree of output offset of the amplifier and the input switching module will occur due to changes of time, temperature, and aging. To correct for these changes, Input Bias Nulling circuits are provided (Figure 6B-2). The A1/A2 PCB also includes autozeroing circuitry that provides dynamic amplifier zeroing during the retrace portion of RF OFF DURING RETRACE (preferred) mode of operation. As shown in Figure 6B-1, Input Signal (Offset) Nulling circuitry is also included for use in the RF ON DURING RETRACE mode of operation.

a. Input Bias Nulling

Input bias currents, due to the switching FETs and the amplifier chain input connections, are small but significant for low level corrections. Correctional offsets for each channel are derived from floating 12 volt supplies and preset by R109 and R112. Refer to the block diagrams (Figures 6B-1 and 6B-2) and the schematic (Figure 6B-3). The 0 VOLT REF for these circuits is driven from the common mode voltage present on the input signal from the external detector/autotester (via U1).

Input Bias Nulling is performed during the one off Nulling process invoked, periodically, by the operator. During this process, all external inputs to the front panel Channel A/B connectors are removed (open).

b. Autozeroing Null

The preferred method of zeroing is with the RF output from the sweeper turned off during retrace, with the output of the detector/autotester still connected through the input module. In this state, the autozeroing circuit described below can null out residual thermal noise up to the point of the detector and, in addition, can zero out a certain level (approximately –40 dBm) of wideband noise from the sweeper.

The Autozero DAC circuit is comprised of U7, which is controlled by latched outputs from U8, U9, and U10. The output of U7 is adjusted by the instrument processor writing correction values to the 10-bit digital to analog converter (DAC) U7. Six bit latches, U8, U9, and U10 latch the data for the DAC. Because the data bus is only 8-bits wide, the most significant 8-bits are latched onto U8 and U9, followed by the remaining 2-bits onto U10. The reference voltage to DAC U7 is set by divider R82 and R101, and is approximately 75 mV. The current output of the DAC is converted to voltage by one half of the dual operational amplifier U6. It is then doubled and offset by the reference voltage (by the other half of U6). Hence, the output of the autozero circuit can be varied between approximately ±75 mV in 1024 steps. This variable autozeroing voltage is applied to the output offset voltage pin of instrumentation amplifier U1, thus enabling any residual output offset voltage from the amplifier chain to be corrected.

c. Input Signal (Offset) Nulling

The Input Signal Nulling circuitry is another form of autozeroing circuitry that is used when the 561 is being used in the RF ON DURING RETRACE mode of autozeroing. During this mode, the sweeper RF power is not being turned off during retrace, so there is a non-zero output voltage from the external detector/autotester; therefore, the residual offset voltages from the amplifier chain must be nulled by another means.

To use this mode of operation, the LOW LEVEL TRIM procedure must first be selected from the front panel calibration menu.

When this operation is selected, the operator is instructed to remove the RF power input to the detector/autotester. The output of the detector/autotester is switched through to the amplifier chain input for autozeroing by DAC U7, just as it would be when zeroing with RF OFF DURING RETRACE mode of operation.

The input switching module switches a short circuit to the input of the amplifier chain and injects offset nulling signals for Channels A/B from DAC circuits U25 and U26.

Without varying the autozero data, the null circuit is used to apply offsets to the input module circuitry to make the noise floor identical to that achieved from the detector/autotester in the RF OFF DURING RETRACE state. Thus we now have an artificial reference with which to compare the output of the amplifier chain for autozeroing during the RF ON DURING RETRACE mode of zeroing.

6B-1.4 Smoothing Filter

The smoothing filter consists of a simple, switched, passive RC filter network. This circuit is comprised of R48 and one (or none) of capacitors C32, C33, C34, and C35 as selected by quad FET switch U5. When *no* smoothing is selected from the instrument front panel, no smoothing capacitance is used and the frequency response is that set by the preceding linear

amplifier stages. If *minimum* smoothing is selected, then capacitors C33 and C34 provide the extra filtering (C34 for channel A and C33 for channel B). The use of individual switching capacitors for each channel avoids lengthy recovery times. If *maximum* smoothing is selected, the extra filtering is provided by capacitors C32 and C35 (C32 for channel A and C35 for channel B).

This 6 bit latch sets the level of smoothing of the signal channel. To avoid lengthy recovery times, separate smoothing capacitors are provided for each of the two multiplexed inputs of each signal channel. Additionally, this latch controls whether the signal channel's input module is switched to the dummy detector position or to the actual detector input.

6B-1.5 Multiplexing and Sample/Hold

The dc voltage output from the signal channel linear amplifier chain is fed to sample/hold amplifier U13 via a five way multiplexing circuit consisting of 4-pole FET switches, U11 and U12. The first position of the multiplexer circuit is used to switch the (multiplexed) channel A/B signal from the smoothing filter to the input of U13. The other four positions of the multiplexer are used to switch in log conformity and temperature voltages from the detectors/autotesters to the sample and hold circuit. The five select lines to the multiplex circuit, and the sample/hold control line for U13 come from the A3 Signal Channel Interface board. C36 is the hold capacitor for U13. The output of the sample/hold amplifier is routed via the board edge connector to the A3 Signal Channel Interface board.

6B-1.6 Log Conformity/Temperature Resistor Sensing

Correction for the log conformity and temperature of the detector/autotester is performed in the 561 instrument software using the information available from the log conformity resistor and thermistor contained within them. The values of these resistances are converted to voltages by connecting them to form voltage dividers. The voltage dividers are connected across a 5.6V reference voltage created by zener diode CR9. The output voltage from each divider is fed via a unity gain, high impedance buffer consisting of a section of the quad op-amp U19, to the five way multiplexer described above. To acheive the high accuracy required in the case of the log conformity reading, preset potentiometers R62 and R64 are included in the log conformity potential dividers; R62 provides adjustment for channel A and R64 provides adjustment for channel B.

6B-1.7 Power Supplies

The ±15V and the +5V supplies to the A1/A2 Signal Channel Amplifier boards are filtered locally on the board by LC π network filters to give increased immunity to noise.

The +5V supply to U2, U5, U11, and U12 is derived from the +15V supply by voltage regulator VR1. This gives increased decoupling over the alternative of using the potentially noisy digital +5V supply.

6B-1.8 Digital Decoding Circuitry

Most of the control signals from the CPU (A5) PCB that control the Signal Channel Amplifier (A1/A2) PCBs are sent via the A3 PCB onto the Quiet Data Bus to latches contained on the A1/A2 assemblies. Signal data activity on this bus is managed so that there is minimum disturbance to the sensistive analog circuitry of the A1/A2 PCB during actual signal measurement.

The remainder of the digital control lines for the A1/A2 PCBs are decoded on the A3 Signal Channel Interface board, from processor bus signals. This decoding is considered in more detail in the description of the A3 PCB.

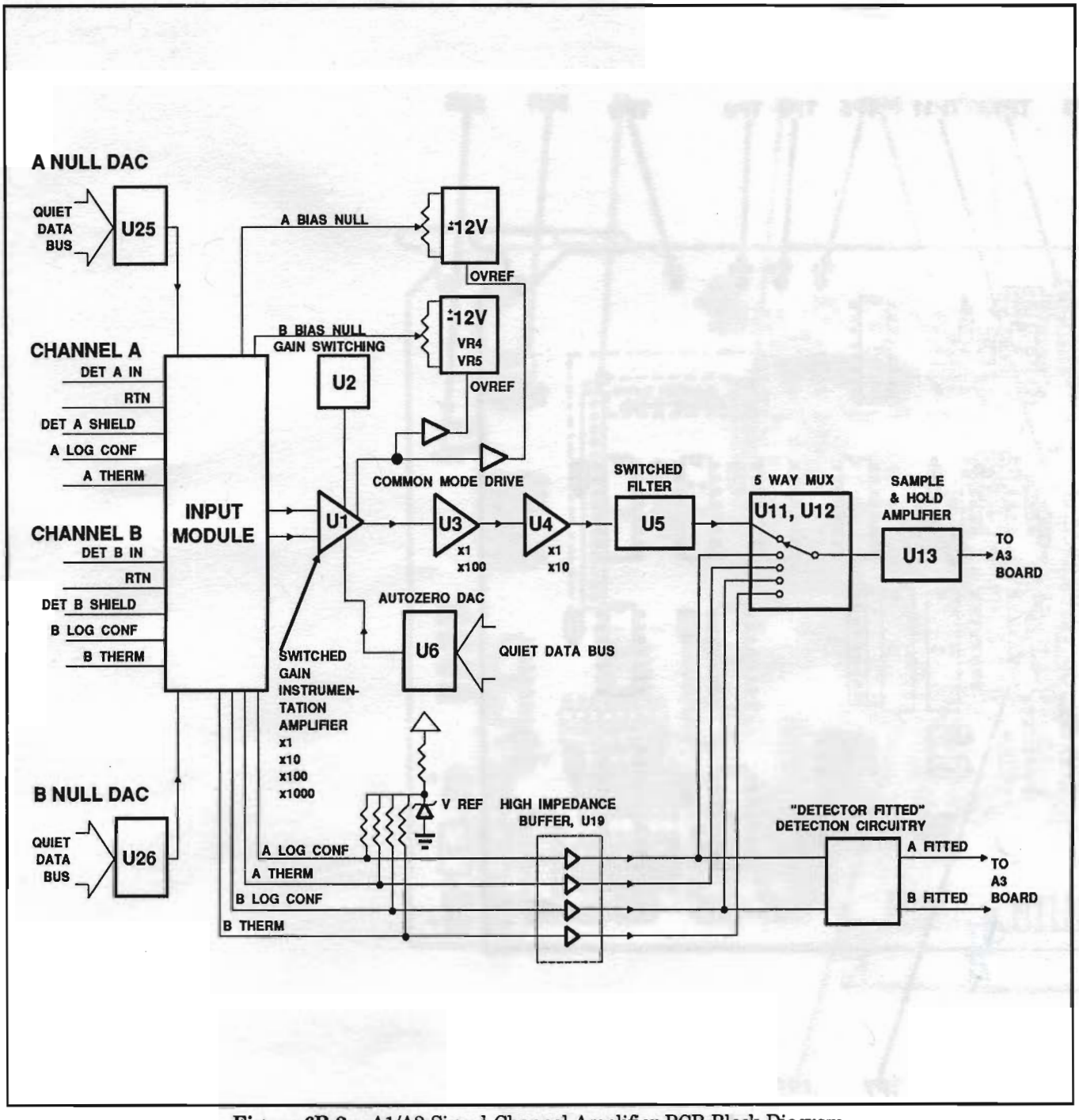

Figure 6B-2. A1/A2 Signal Channel Amplifier PCB Block Diagram

6-10 6B

6C-1 A3 SIGNAL CHANNEL INTERFACE PCB FUNCTIONAL DESCRIPTION

The 561 Scalar Network Analyzer contains one signal channel interface PCB (A3). This PCB contains decoding circuitry to control the various functions of the A1 and A2 signal channel amplifier PCBs, and performs the analog to digital conversion of the signals from these PCBs for interfacing with the instrument CPU PCB.

The A3 PCB also contains an analog channel that is used to digitize the 10V sweep ramp signal from the A4 sweeper interface PCB. Refer to the block diagram (Figure 6C-1), the parts locator diagram (Figure 6C-2), and to the schematic (Figure 6C-3) located on the fold-out pages.

6C-1.1 Input Multiplexing Circuit

Analog signals from the signal channel amplifier (A1/A2) PCBs and the ramp output of the Sweeper Interface (A4) PCB are input to the edge connector of the Signal Channel Interface (A3) PCB. Two quad FET switch integrated circuits, U1 and U2, are configured as a multiplexing circuit to select the desired analog signal. The sense and return paths of each signal are arranged so as to be switched through the same switching integrated circuit (ie. U1 or U2) in order to acheive a similar series resistance within the input path, so as to maintain the common mode rejection characteristics of the following differential amplifier stage (U3).

The fourth multiplexing switch position is connected to the circuit analog ground. This position is used during instrument self test to inject a reference offset at the input of the analog to digital converter so that its operation can be verified.

The plus 5V supply for U1 and U2 is derived from the plus 15V supply using the three terminal voltage regulator VR2. This technique helps to decouple this circuitry from the potentially noisy digital 5V supply. The input multiplexing circuit is switched by U17, an octal latch, and the state of these four control lines can be monitored by probing test points TP11 to TP14. These test points correspond to the analog input signals as shown in Table 6C-1.

6C-1.2 Op-Amp Stages, U3 and U4

U3 is a x1 gain operational amplifier chosen for its low noise and low offset voltage characteristics. It is configured in the elementary single op-amp differential amplifier circuit to acheive common mode rejection between the signal channel interface and the circuits feeding it.

The output of U3 goes to U4, a x1 gain inverting buffer stage. This stage inverts the negative going signal at the output of U3 in order to present the ADC, (analog to digital converter), with a positive going signal (the ADC is configured in its unipolar mode of operation). U4 also presents the ADC input with a low driving impedance that is necessary to avoid modulating the ADC input at high frequencies. In order to ensure that the signal at the ADC input is actually positive, even when small negative offsets are present, on the multiplexed input signals, an offset voltage of 50 mV is applied to the non-inverting input of U4. This voltage is set by the potential divider R14 and R7 connected across the voltage source formed by the zener diode CR1. An offset applied to the op-amp terminal in this way will result in a voltage actually applied to the ADC input of 2 x V offset, ie. 100 mV.

6C-1.3 Analog to Digital Conversion

The analog-to-digital conversion circuit (ADC) is comprised of U6, a 12 bit resolution device that is configured to accept an input voltage range of 0 to 10V. This device requires a plus and minus 15V supply, as well as a plus 5V supply. In this case the +5V supply is derived from the plus 15V supply rail using VR1, a three terminal voltage regulator. The ADC conversion process is initiated by the STROBE ADC NIBBL signal from U10, the eight line decoder integrated circuit.

The 561 CPU (A5) PCB communicates with the signal channel interface PCB over an 8-bit data bus; therefore, the 12-bit output of the ADC requires two separate read operations. First, the octal tri-state buffer, U7, is enabled by a decoded line from U10 to read the eight most significant ADC data bits, D11 to D4. Then octal tri-state buffer, U8, is enabled by another decoded line from U10 to read the four least significant bits of ADC data, D3 to D0. These appear on the 561 data bus bits D7 to D4 respectively.

The other four sections of buffer U8 are used for the A1 PCB fitted data bit; the output of the detector fitted latch; the status of the synchronised sample/hold latch; and the status of the ADC. These functions are described in more detail later under their appropriate sections.

6C-1.4 Sample/Hold Control Circuit

The signal channel interface PCB outputs a common sample/hold control line to the sample and hold amplifiers contained on the signal channel PCBs. The actual sample/hold signal can be derived in one of two ways.

The primary way is to allow the CPU to directly set the sample-and-hold signal as and when it is required to. To do this, pin 2 of U17 is set high, thus presenting a logic 1 to one input of the two input OR gate, U15A. Hence, the output of this gate will be a logic 1 regardless of the level of its other input. The logic 1 output of U15A is presented to one input of the two input AND gate, U13A. This gate is then effectively enabled and its output follows the state of its other input which is derived from the output of one of the D type latches contained within U20.

The output of U13A is the sample/hold signal and is also set high or low (high for sample, low for hold) by writing to the latch contained within U20 using the decoded line from from the eight bit decoder U10, and the data bit D0. The other way of controlling the sample/hold signal is to synchronise the holding of a signal with the rising edge of the instrument cathode ray tube (CRT) horizontal synchronisation pulse. This is particularly advantageous for low level signal channel signals. Shortly after the edge of the pulse, a large interfering pulse is radiated from the CRT. This could affect the accuracy of the signal being read if the channel was still sampling data at that time.

6C-1.5 Detector Fitted Circuitry

As shown in Figure 6C-1, each signal channel amplifier feeds status information to the A3 Signal Channel Interface PCB pertaining to whether detectors are connected to the instrument front panel and whether the signal channel PCB is plugged into its edge connector. All these signals arrive at the signal channel interface PCB, and all but one are read using octal buffer U18. This buffer is read using a decoded output from the eight line decoder U9. The remaining signal, the one that tells whether the A1 PCB is fitted, is read over one of the spare data bits of octal buffer U8.

In addition to being fed to buffer U18, the DETECTOR FITTED signals are latched by latches U19, U21 and U22. The outputs of these latches go to the 6-input OR gate formed by U16A, U16B, U16C, U16D and U15b. Thus if any of these latches is tripped, a high logic level occurs at the DETECTOR FITTED output of the OR gate and is routed to one of the spare bits of the octal buffer U8. This signal is read by the CPU, along with the least significant four data bits from the ADC. Because of the DETECTOR FITTED signal, the CPU does not have to continuously poll buffer U18 to see when a new detector/autotester has been inserted at the front panel. This signal remains high until the latches U19, U21 and U22 are reset by the CPU by pin 5 of latch U17.

6C-1.6 Signal Channel Multiplexer Control

Five outputs of the octal latch, U11, are used as control signals for the five way multiplexer contained on each signal channel amplifier PCB. These control signals are paralleled to each PCB, so that the multiplex circuits are switched at the same time.

6C-1.7 Quiet Data Bus

Octal buffer U12, is enabled by any one of the signal channel select lines from U9 via AND gate U5. In this way, the noisy CPU data bus is only connected to the signal channel PCBs when it is required to write to them. Thus, the sensitive analog circuitry contained on the signal channel amplifier PCBs is isolated from the general background noise level of the instrument data bus.

6C-1.8 Power Supplies

The plus and minus 15V and the plus 5V supply rails to the A3 Signal Channel Interface PCB are all filtered locally on the PCB by LC pi-network filters to obtain increased immunity to noise. Voltage regulators VR1 and VR2 locally regulate from the +15V supply to provide +5V supplies to the analog function integrated circuits, U1, U2 and U6.

6C-1.9 Digital Decoding Circuitry

The digital control lines for the A3 signal channel interface and the A1/A2 signal channel PCBs are decoded from CPU control lines by the two eight line decoder integrated circuits U9 and U10. Some further decoding is implemented on the signal channel PCBs themselves using a combination of the CPU control lines and the PCB select line from the A3 PCB.

6D-1 A4 SWEEPER INTERFACE PCB FUNCTIONAL DESCRIPTION

The purpose of this PCB is to provide an interface for the control signals that operate between the 561 and its associated sweeper signal source. All the signals required to allow the 561 to operate with a wide range of sweepers are provided. The PCB contains both analog and digital circuitry which are physically separated. However, it is more logical to consider the whole as a series of functional units; some of containing analog circuitry, containing digital circuitry, and some containing both analog and digital circuitry. Refer to the block diagram (Figure 6D-1), the parts locator diagram (Figure 6D-2), and to the schematic (Figure 6D-3) located on the fold-out pages.

6D-1.1 10V Reference

Op Amp U1, diode CR1, and resistors R1, R2, and R3 form a 10V reference voltage source. CR1 is in fact an IC with the characteristics of a very high- grade 5.0V zener reference diode. U1 provides buffering and a gain of 2 to produce an output voltage of approximately 10V, which is stable over time and temperature. Stability is further improved by providing the current for U1 from the output of the Op Amp. The Op Amp is powered from a single +15V supply to ensure that the reference always starts up in the positive direction.

6D-1.2 Digital to Analog Converter

ICs U22, U23, and U24 form a 12-bit digital to analog converter. This circuit is used to produce the operating reference voltage for the sweep ramp comparator circuit.

The output of U24 (negative) is a fraction of the 10V reference voltage. The actual value is determined linearly by the magnitude of the 12-bit data word loaded into U23 from the CPU. Since the data bus is only 8-bits wide, U22 is required to temporarily store the lower 4 bits of the data word. This word is loaded seperately prior to loading U23. Its output, together with the 8-bit data bus, then forms the 12-bit data word required.

6D-1.3 Sweep Ramp Normalizer and Detection Circuit

Resistors R4, R5, R6, R7, R8, R77, and IC U2A form an inverting, differential input buffer amplifier with an overall gain of approximately –0.77. The gain of the feedback loop around the Op Amp itself is –1; however, attenuation is provided by resistors R4 and R6. This attenuation is necessary to allow the use of some sweepers with sweep ramps of magnitude greater than 10V. Resistors R9, R10, R11, R12, R13, and IC U2B form a x1 gain inverting amplifier with a small amount of output offset. An offset voltage, set by R12 and R13, is introduced to allow for a possible negative offset on the input ramp signal. Note that although the gain at the inverting input of U2B is 1, the gain at the non inverting input is 2.

Therefore the offset voltage set by the resistors is amplified by a factor of 2. This offset provides an under voltage range of approximately 1V. A potentiometer, R10, is included in the feedback loop of U2B to allow adjustment of the overall gain of the two stages. IC U3 is a Sample and Hold Amplifier whose output is connected via the motherboard to the Signal Channel Interface (A3) PCB. This provides an alternative method of tracking the sweep ramp input. IC U4 is a high speed, precision voltage comparator. Its purpose is to monitor the voltage resulting from the summation of the normalised ramp voltage and the DAC voltage and to set a flag when this resultant voltage is zero.

The tracking of the sweep ramp happens in the following manner: the desired voltage level corresponding to a data collection point is loaded into the DAC. The negative voltage output from the DAC is then summed, via R16, with the positive ramp voltage from U2b via R15. Since, at this stage the magnitude of the ramp voltage will be less than than that of the DAC voltage, the resultant will be negative. This will cause the output of the comparator to be at logic low (TTL levels). As the ramp voltage rises the summed voltage becomes less negative until the ramp voltage is equal in magnitude to the DAC voltage whereupon the summed voltage will be 0V. At this point the comparator triggers and the output goes to logic high (5V). This signal passes via U25a to U11d. From there it passes to the status register, U21, and to open collector driver U14a. This driver then forces the /DWELL output low and stops the sweeper. The whole system remains in this state whilst a measurement is taken. The /DWELL line is released by loading the next higher data collection point into the DAC. The output of the comparator then goes low and the whole process is repeated until the end of the sweep. U25a is used to invert the sense of the comparator output so that the ramp voltage can be tracked during both forward sweep and retrace phases. Gate U11d whilst inverting the ramp comparator output can also be used to enable

and disable the /DWELL line being controlled by the ramp comparator. /DWELL itself can also be set independantly from the control register via gate U13b. Resistor R18 provides the ramp comparator with hysteresis by positive feedback.

6D-1.4 Sequential Sync Normalization

The Sequential Sync line provided by some sweepers may combine frequency marker pulses as well as the various blanking pulses. This circuit is designed to seperate the marker pulses, if they are present, from the blanking pulses. For this circuit to operate correctly the blanking pulses must be positive and the marker pulses must be negative. Resistors R31, R32, and IC U6 form a x1 gain, inverting buffer. Negative pulses from the output of this buffer (i.e., blanking pulses) are passed via a level translator, R39, R40, and CR9, to gate U11C. The output from this gate is Composite Blanking. It is routed to the status register and, via U15b, to flip flop U17A. The output of U17A is OR'ed with several other signal lines to form the interrupt line /INT7.

Any positive pulses at the output of U6 are fed via R33 and CR8, which block negative signals, to voltage comparators U7C and U7D. U7C has a threshold voltage of 3V and detects Marker pulses. U7d has a threshold voltage of 6.5V and detects Active Marker pulses. Apart from the difference in thresholds the action of the two circuits is identical therefore only the Marker circuit will be described. Device numbers for the Active Marker circuit are shown in brackets.

The output of the comparator remains off and is pulled high by R37 (R43) until the input signal exceeds the threshold voltage. At this point the comparator turns on and its output goes low. R38 (R44) provides positive feedback for hysteresis to increase noise immunity. The comparator output goes to gate U11A (U11B) where it is conditioned. From there it goes to the clock input of flip flop U16A (U16B). The output of the flip flop goes to the status register and to gate U15D where it is OR'ed with other signals to produce /INT7. R34 ensures that the signal inputs of the comparators do not float up past the thresholds when no signal is applied.

6D-1.5 Video Marker Normalizer

This circuit provides an alternative means of inputting frequency marker information for those sweepers which have a seperate Video Marker output. It does not differentiate between Active and non Active markers. However, it will accept both positive and negative marker pulses. Resistors R19, R20, zener diodes CR2, and CR3 provide overvoltage protection to the non inverting, x1 gain buffer formed by U5A. The protection circuit limits the voltage applied to the buffer to a maximum of approximately +/–10V. The output of buffer U5A is taken via the inverse parallel connected diodes CR20 and CR21 to a high gain, inverting amplifier stage whose output voltage is limited to about 5.1V. This is formed by U5D,

R21, R22, R72, CR4, and CR5. This stage converts an input pulse of whatever shape or amplitude to a 5.1V square wave pulse of opposite polarity. Since this stage has high gain (around 50), even small signals at the input will produce 5.1V pulses at the output. This includes noise. The two diodes CR20 and CR21 block signals of less than about 0.6V thus reducing the likelihood of spurious output pulses due to low level noise.

Resistors R23, R24, R25, R26, R27, and R28. Diodes CR6 and CR7, and Op Amps U5C and U5D form a Full Wave Rectifier or Absolute Value circuit which has an overall gain of +/–1. A signal of either polarity applied to the input will appear at the output with the same polarity but with a fixed, positive polarity. The purpose of this circuit together with the two preceeding stages is to convert input marker pulses of any shape size or polarity, within certain limits, to uniform, 5.1V, square-wave pulses of positive polarity.

The marker pulses from the absolute value circuit are detected by a comparator, having a threshold voltage of approximately 3V, formed by U10C, R30, R74, R75, and R76. The output of this comparator goes low (0V) when the input exceeds the threshold otherwise it is held high (5V) by R29.

Hysteresis is provided by R74. The output of the U10c is OR'ed into the Sequential Sync circuit by gate U11A.

6D-1.6 Retrace Blanking and Bandswitch Blanking Normalizer Circuits

The Retrace and Bandswitch Blanking Normalizer cicuits are identical in form and function. Therefore only the retrace circuitry will be described. Corresponding Bandswitch circuit component numbers appear in brackets. Resistors R45, R46 (R55, R56), zener diodes CR10, and CR11 (CR14, and CR15) form an input protection circuit limiting, to

approximately +/–10V, the signal applied to the x1 gain, non inverting buffer formed by U8A (U8B).

The output of the buffer is connected to an Absolute Value circuit consisting of R47, R48, R49, R50, R51, CR12, CR13, U9B, and U9A (R57, R58, R59, R60, R61, CR16, CR17, U9C, and U9D). The action of this circuit is identical to that of the Absolute Value circuit described in the Video Marker section above.

The output of the Absolute Value circuit is monitored by the voltage comparator circuit U7A (U7B). This has a threshold voltage of approximately 2.5V fixed by R52 and R53 (R52, R53). The output of this comparator goes low (0V) when the input exceeds the threshold otherwise it is pulled high (5V) by R54 (R62). The comparator output is routed via gate U12A (U12B) to the status register.

The outputs of gates U12A and U12B, in addition to being routed seperately to the status register, are OR'ed together by gate U15A. The resulting composite signal is then OR'ed with the Composite Blanking signal from the Sequential Sync circuit by gate U15B.

6D-1.7 Alternate Sweep Normalizer Circuits

The Alternate Sweep Enable Normalizer and Alternate Sweep A/B Normalizer circuits are identical. Therefore only the Enable circuit will be described. A/-B circuit component numbers are shown in brackets. The input signal is fed via resistor R63 (R66) to a voltage comparator U10A (U10B) whose threshold voltage of approximately 2.5V is set by resistors R52 and R53 (R52, R53). Resistor R64 (R67) prevents the comparator's signal input from floating above the threshold voltage when no signal is applied. The comparator output goes low (0V) when the input exceeds the threshold otherwise it is held high (5V) by R65 (R68). This signal goes, via gate U12D (U12C), to the status register.

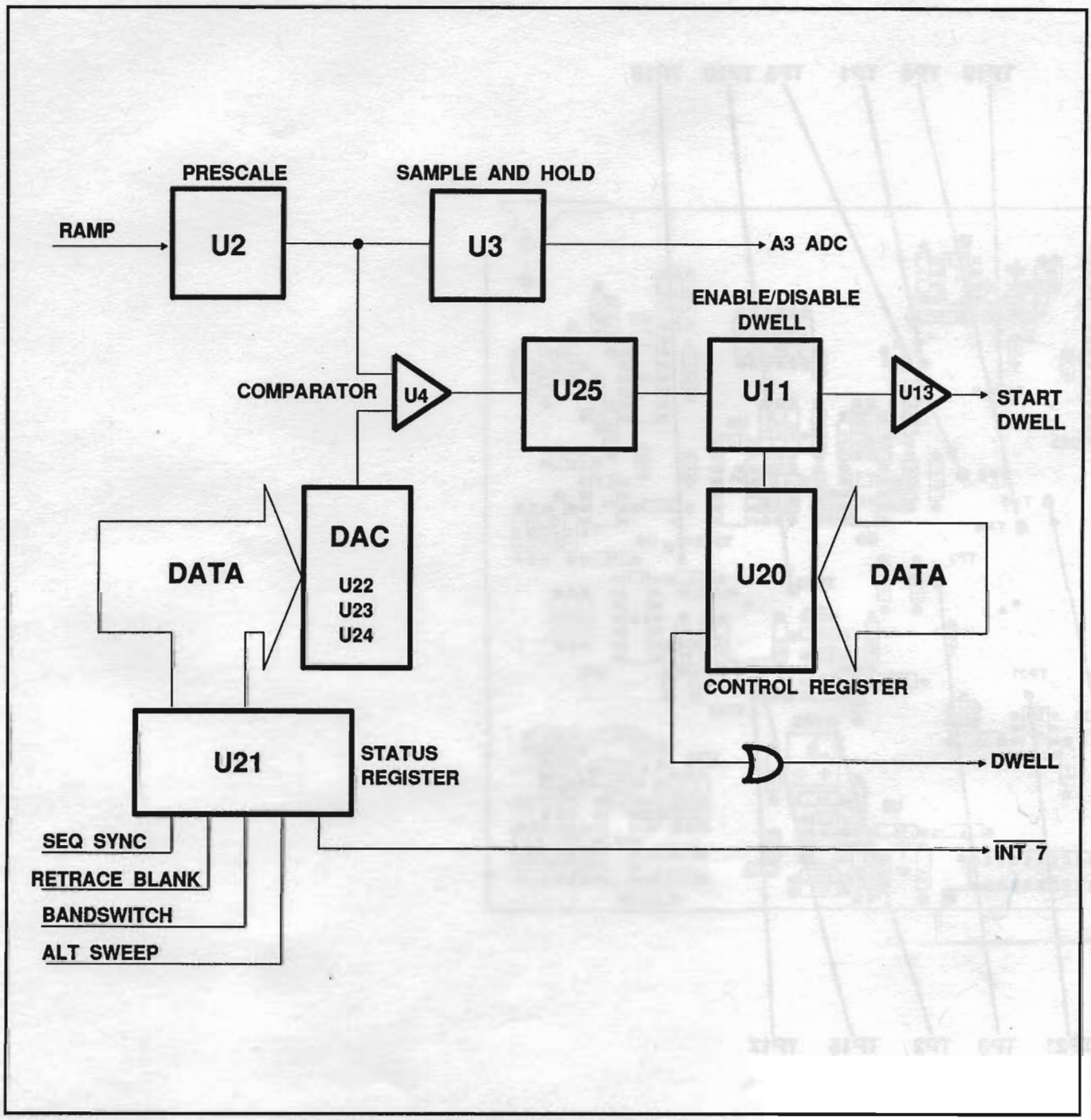

Figure 6D-1. A4 Sweeper Interface PCB Block Diagram

6E-1 A5 CENTRAL PROCESSOR UNIT PCB FUNCTIONAL DESCRIPTION

The A5 Central Processor Unit PCB performs all control functions for the 561. It controls the A4 Sweeper Interface PCB and the A1/A2 Signal Channel PCBs (indirectly) in order to perform measurements and to send the resultant data to the graphics subsystem (A6/A7) for display. All other PCB control functions, including those for both GPIB PCBs, are performed by the A5 PCB; refer to the A5 processor memory decoding block diagram (Figure 6E-1), the A5 PCB block diagram (Figure 6E-2), the parts locator diagram (Figure 6E-3), and to the schematic (Figure 6E-4).

6E-1.1 Processor / Memory / Decoding

The microprocessor chip, included on the A5 PCB, is the IAPX88/10 (8088). It is used in the MIN mode with a clock frequency of 8 MHz. This clock signal is derived from the 24 MHz crystal Y1 and the clock controller chip U2, which also takes care of the power up reset through R1, C1 and CR1. U3 provides a signal, derived from the processor I/O/M line and the ALE line, that is inverted through U13. This causes U2 to force the processor U1 to execute one wait state whenever an I/O port is selected.

As the address lines on this processor are multiplexed with the data lines and the status lines it is necessary to latch them with U4, U5 and U27, data bus buffering being provided by U28. The high order address lines are fed to U7 along with the I/O/M line where they are decoded to give the eight memory select lines /MSEL0 thru /MSEL7. This provides 256K Bytes of decoding at 32K Byte boundaries. As the two most significant address lines are not used the memory map repeats itself four times in the total map. This feature is necessary as the processor resets to address FFFF:0000, which is at the top of the map. This allows execution of the reset vector from an image of the last EPROM thus being directed into the actual code.

6E-1.2 Input/Output Ports

Input and output ports are decoded into groups of 16 by U11 from address line 4, 5 and 6 and I/O/M. These I/O selects are bussed throughout the instrument, via the Motherboard, and used as PCB select lines.

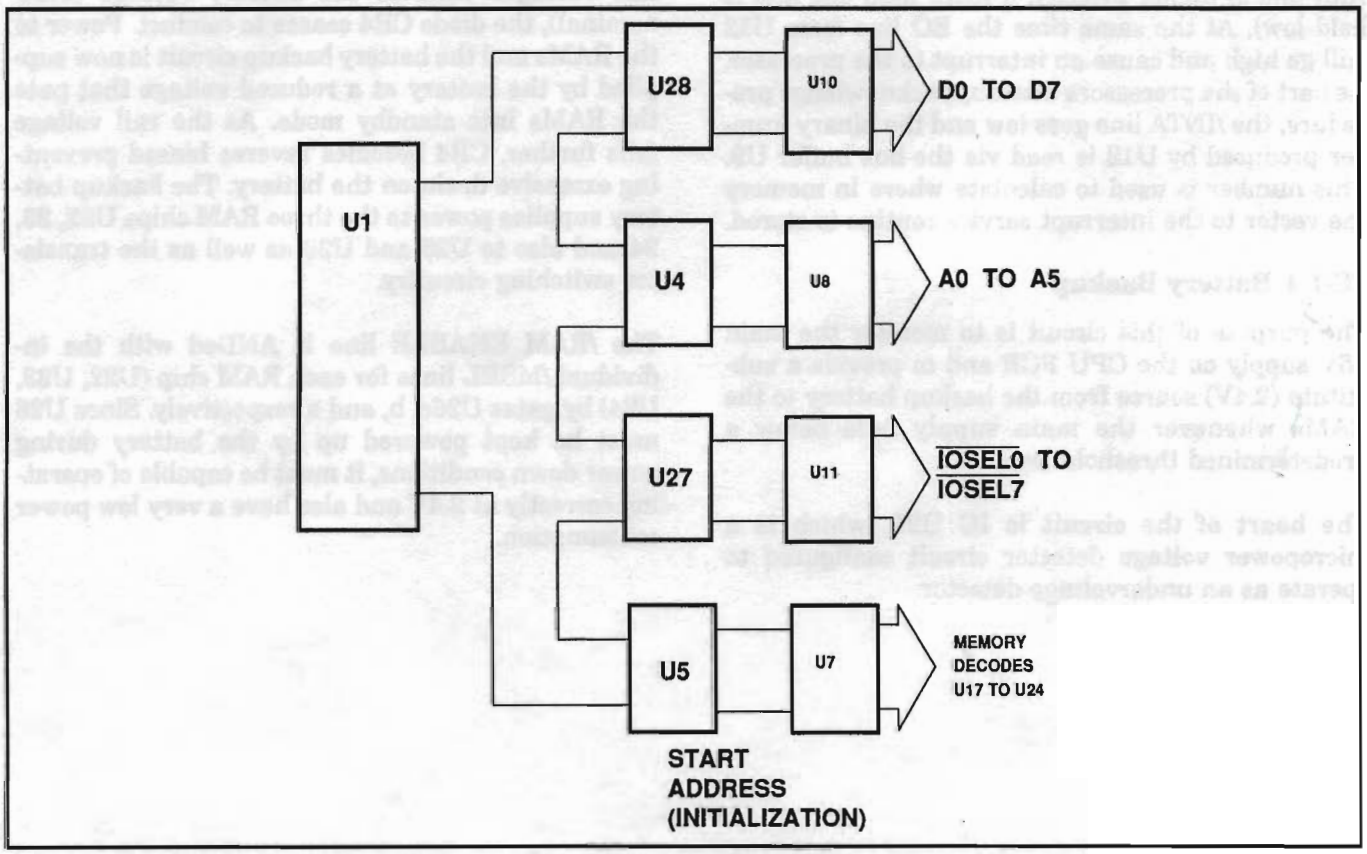

Figure 6E-1. A5 PCB Processor Memory Decoding Block Diagram

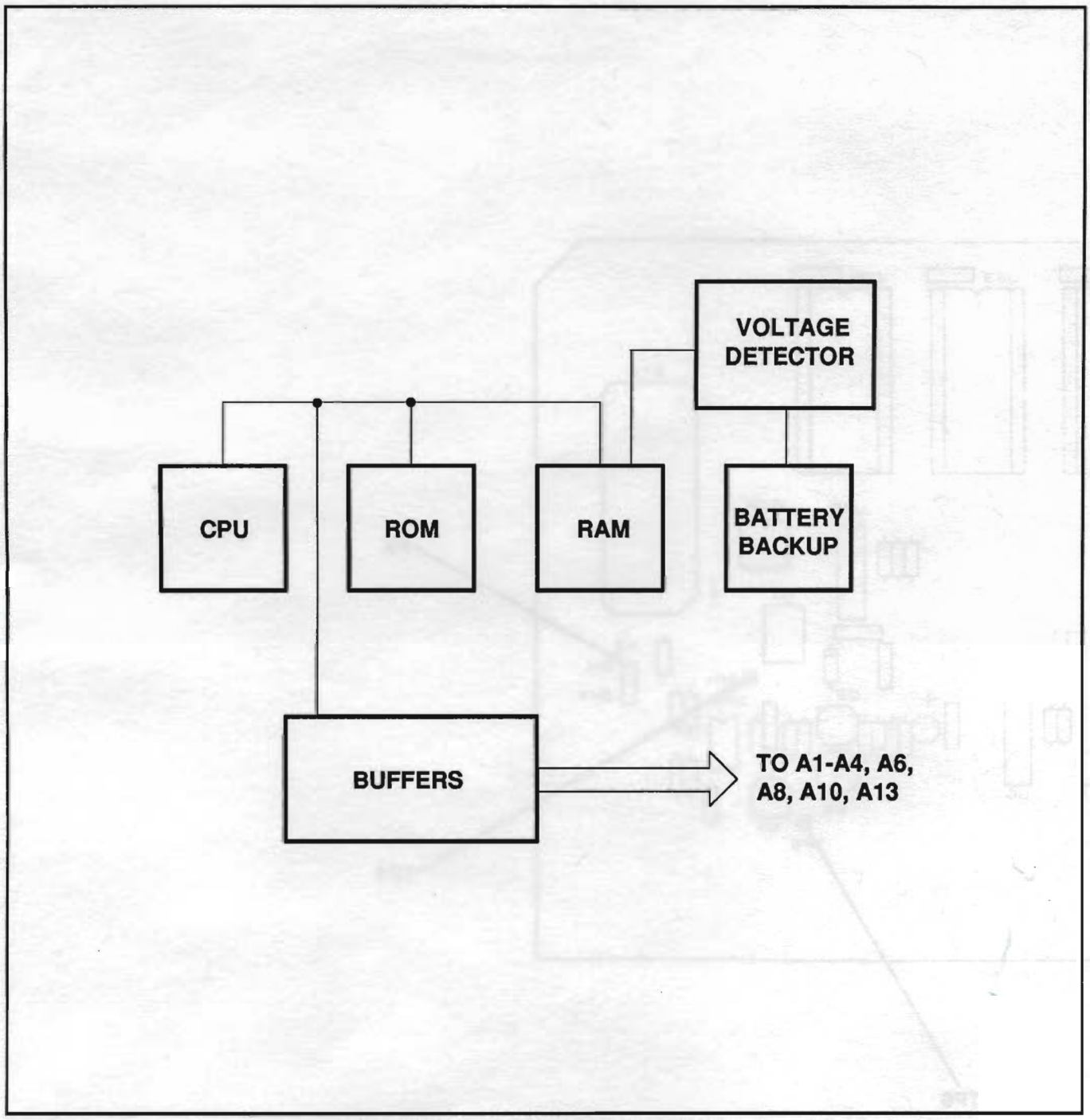

Figure 6E-2. A5 CPU PCB Block Diagram

6F-1 A6 TEXT AND GRAPHICS PROCESSOR PCB FUNCTIONAL DESCRIPTION

All of the 561 display and printer control functions are performed by the graphics subsystem, which is comprised of the A6 Text and Graphics Processor PCB and the A7 Video Display Processsor PCB (VDP). The main processor board does not interface directly with the A7 PCB; all A5/A7 data transactions are handled via the A6 PCB.

The A5 Central Processor Unit PCB treats the graphics subsystem as an intelligent terminal and sends it measurement display data as a combination of ASCII text and escape codes. Much of this data requires further processing, such as the addition of hexadecimal data codes for the printer output. Refer to the block diagram (Figure 6F-1), the parts locator diagram (Figure 6F-2), and to the schematic (Figure 6F-3) located on the fold-out pages.

6F-1.1 Processor / Memory / Decoding

The microprocessor chip, U1, is the IAPX88/10 (8088); this chip is used in MIN mode with a clock frequency of 8 MHz. This clock signal is derived from the 24 MHz crystal Y1 and the clock controller chip U6, which also performs the power up reset function through R1, C4 and CR1.

The address lines used with this processor are multiplexed with the data lines and the status lines; therefore, it is necessary to latch these lines with U7 and U23. The high order address lines are routed to U8 which, with the IO/M signal, provides the memory decode signals /MEMS0 thru /MEMS3. These provide decoding of the first 128 Kbytes at 32 Kbyte boundaries. A section of U22 is used to provide additional mapping of /MEMS1. (This is the top EPROM site.) When the 8088 is reset, the registers are loaded to begin execution at FFFF:0000 and the additional decode ensures that an image of the /MEMS1 prom appears at the top of the map. The last 16 bytes of this prom contain the vector address to the start of code; after the processor has jumped there, execution can carry on normally.

The main CPU PCB communicates with the graphics subsystem through a dedicated 8-bit parallel communications interface referred to as the PIPE. When the CPU sends information to the TGP it is latched into U13. The latching of this data will cause either one half or the the other of U15 to toggle. This status can be read by the TGP through U11B to determine if the byte sent is to be interpreted as command or data, and can also be read by the CPU through U11A to find if the byte has been accepted. Reading of the latch by the processor will cause U15 to be reset and ready to receive the next command or datum.

Should the CPU request the TGP to send data then the TGP will latch the datum into U14. The action of latching the byte will cause U17 (pin 5) to become active, thus providing a data available status through U11A for the CPU to monitor. The action of reading the latch will clear the status. As the TGP also monitors this status through U11B, it will knew when the byte has been accepted by the CPU.

The line frequency TICK signal is made available to the TGP processor through U11B. This input does not affect the operation of the PIPE but is provided so that the processor can measure the line frequency and correctly set up any line frequency sensitive parameters.

6F-1.2 Hardcopy

The hardcopy system provides a software buffer of approximately 50K bytes, that is emptied under interrupt, and Centronics interface driver hardware.

These hardcopy functions are implemented by U18, the decoder that is used to select the various modes of these operations.

6F-1.3 Centronics Status Port

To send data to the Centronics port, the TGP processor first reads the status port to see if the printer is busy. One half U21 is used as a 4 bit input port to report on the centronics status. If the printer is not busy, the data to be sent is loaded into the data latch U20. This data is then presented to the printer through the buffer U25. To signal to the printer that the data is available, a strobe pulse must be generated. This is done by first presetting U24A and then clearing it. The /Q output is buffered by the

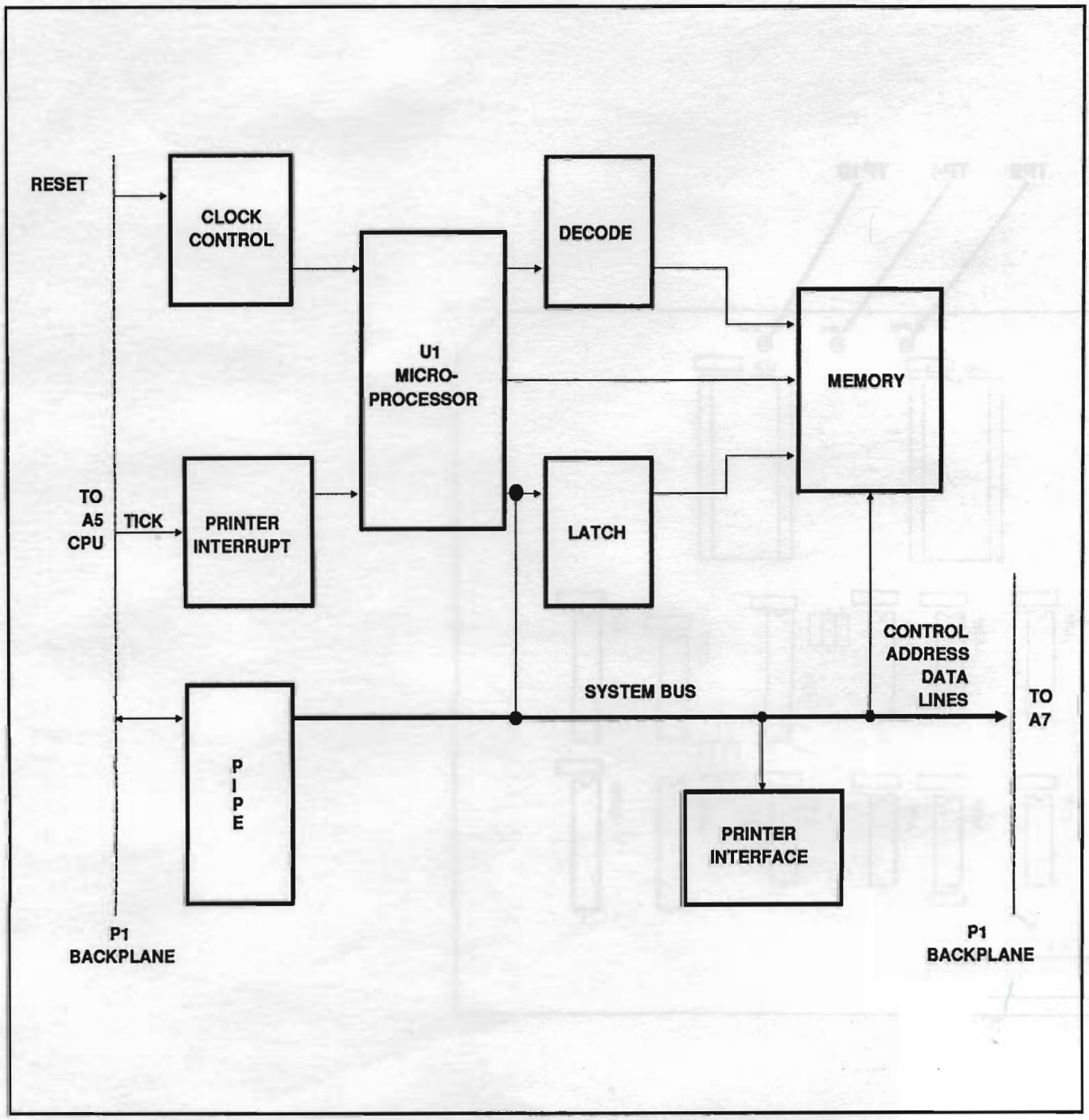

Figure 6F-1. A6 Text and Graphics Processor PCB Block Diagram

6G-1 A7 VIDEO DISPLAY PROCESSOR PCB FUNCTIONAL DESCRIPTION

The A7 Video Display Processor PCB is to takes raw data (i.e., the information to be displayed and screen coordinate information) from the Text and Graphics Processor (A6) and transfers it, suitably processed, to the internal and external monitor.

The A7 PCB consists of a dedicated Graphics Display Processor chip (GDP), control and timing logic, video driving circuitry, and three identical blocks of memory, hereafter referred to as video memory planes. Refer to the block diagram (Figure 6G-1), the parts locator diagram (Figure 6G-2), and to the schematic (Figure 6G-3) located on the fold-out pages.

6G-1.1 A7 PCB Circuit Description

Each plane of the video memory consists of four 16K x 4 bit dynamic RAMs arranged in the form of a 16K word of 16 bits each. Each bit represents one pixel on the CRT display. Therefore, each plane represents an image of 512 x 512 pixels. The images represented by the three memory planes are superimposed one upon the other to produce the displayed picture.

The three planes are designated 0, 1, and 2. Plane 0 holds the image of the alphanumerics, graticule, and markers/cursor. Plane 1 holds the image of the Channel 1 trace. Plane 2 holds the image of the Channel 2 trace. This memory is separate from, and cannot be accessed by, either the A5 Central Processor Unit PCB or the A6 Text and Graphics Processor PCB.

6G-1.2 Graphics Display Processor Chip (GDP)

The Graphics Display Processor chip, U1, generates the necessary signals to produce a raster scanned display upon a CRT monitor. All it requires are high level drawing commands, the data to be displayed, and display coordinates. This information is supplied by the TGP. The VDP is not connected directly to the main CPU. All communications to and from it must be via the A6 TGP PCB.

The GDP chip controls all video timing, maintenance of the video memory (refreshing), memory manipulation and the continuous process of reading out the data for display. The master clock for the VDP PCB, where all video timing is derived, is a voltage controlled oscillator that is synchronised to the mains frequency by a phase locked loop circuit. In this way the perturbations in the display due to line frequency interference are eliminated.

The video and timing signals produced by the GDP are further processed to produce a Composite Video signal for the external monitor and a mixed Video with Blanking and separate Timing signals for the internal monitor.

U1 communicates with the TGP via three 8 bit ports internal to U1. Two of these ports are write-only and the other one is read-only. The two write-only registers are a command register and a parameter register. The read-only register is a status register. The interface, which is controlled by the TGP, consists of an 8 bit bidirectional data bus, PD0 to PD7, an address line, A0, and two direction control lines, /PIOS0 and /PIOS1, which are connected to U1s /RD and /WR inputs respectively.

6G-1.3 Phase Lock Loop/Master Clock Circuitry

As stated above, the master clock is adjusted so that the frame repetition rate, controlled by the VSYNC signal, which is derived from the master clock, is synchronised with the input line frequency. This is achieved by enclosing the voltage controlled oscillator which produces this master clock (i.e., the Dot Clock) within a phase locked loop. The VSYNC signal is compared with TICK, which is a TTL compatible signal obtained from the line input in the power supply. This comparison is performed by the phase detector, composed of a dual J-K flip flop, U12, gate U14d, and resistors R18, R19. This is a type II phase detector which produces positive and negative pulses for lagging and leading phase shifts respectively; it does not produce pulses when the two input signals are exactly in phase. The pulses from the phase detector are fed via a low pass filter network (R20, R21, C2) to an active integrator (U13,R22, C3). Because U12 is an LSTTL device, the output pulses (both positive and negative) are centered about a point midway between the two TTL levels it produces. For proper operation, the integrator inputs must also be biased about this same point. Resistors R23 and R24 achieve this and capacitors C67 and C68 provide extra noise limiting. The output of the integrator is a dc level proportional to the polarity and width of the phase detector pulses.

The voltage controlled oscillator consists of gates U14a,b,c, resistors R28, R29, capacitors C4, C5, C6, C7, radio frequency choke L4, and varactor diode CR4. The fundamental frequency of the oscillator is set by R29 and C6 but it can tuned by applying a dc level across CR4 which exhibits a voltage dependent capacitance. This tuning voltage can be supplied via header P2 either as a fixed voltage from the voltage divider formed by R25, R26, R27 (in which case the Dot Clock frequency is independent of the line frequency and is said to be in Free Run mode) or as a variable voltage from the output of the integrator circuit. For the later case the phase locked loop is closed and the Dot Clock frequency is tuned so that VSYNC is exactly the same frequency as the line.

Components R28, L4, and C4 form a low pass filter which prevents any signal at oscillator frequency being fed back to the output of the tuning voltage source. C5 blocks the potentially large dc tuning voltage (up to 15V) from the low voltage (5V) input of gate U14A.

6G-1.4 CRT Interface

The GDP chip produces the required horizontal (HSYNC) and vertical (VSYNC) synchronisation signals. HSYNC is buffered by gate U18b before being applied to the internal monitor and header P3 allows the selection of inverting or non inverting buffering. The video image is interlaced; two complete scans of the picture area are required to produce the complete image. As a result, the circuitry for VSYNC is more complex. The lines making up the two raster scans are interleaved and to achieve this the VSYNC pulses for every alternate scan of the display are offset in time relative to the other video signals. The GDP provides VSYNC offsetting automatically. However, the method employed can result in an error in this offset of up to 15 percent, which produces unequal line spacing and subsequent vertical jitter in the display. To combat this problem, the VSYNC signal is fed through a correction circuit before being buffered in a similar manner to HSYNC (gate U18c) and then applied to the monitor. The correction circuit consists of flip flops U15, U16, monostable U17, and gates U23A/U24B. This circuit ensures that VSYNC is offset by a precise amount by clocking it through the flip flops with the GDP clock (2xWCLK) and the /RAS line.

The actual inter line spacing appearing on the CRT may be adjusted using R48. Header P4 allows the selection of, inverting or non inverting buffering of VSYNC. The video signal applied to the internal monitor consists of the outputs from the three planes of video memory and a synchronised version of the GDPs BLANK signal called BLANKING. The BLANKING signal is clocked through a flip flop (U10b) by the same signal which clocks the video data from the memory planes (LOAD). This ensures that the BLANKING and VIDEO signals are subjected to the same amount of gate delays and remain in sync thereby preventing spurious data being displayed at the edges of the CRT.

The BLANKING and VIDEO 0, 1, and 2 signals are combined by gates U19a,b,c, and diodes CR1,2,3. This combined video signal is then passed through two stages of amplification provided by transistors Q1 and Q2. This combined amplified video signal is then passed via an emitter follower, Q4, to the internal monitor. The combined video output from Q2 is also mixed with VSYNC and HSYNC signals from gate U18a. The resultant signal, COMPOSITE VIDEO, is buffered by emitter follower Q3 and then presented to a rear panel connector for use by an external monitor.

6G-1.5 Memory Timing

All communication between the GDP and video memory takes place over the 16-bit bus formed by the U1 pins designated AD0 to AD15. This bus carries both data and addresses. It is used to both update and examine video memory and also to control the readout of memory data for display.

To update/examine the video memory, U1 initially places the address on the bus. The upper 8-bits, which constitute the RAM column address are first latched by the /ALE (Address Latch Enable) signal from U1 into latch U4. The lower 8-bits of AD0-AD15 (which constitute the RAM row address) are then multiplexed with the latched column by two quad multiplexors U5 and U6. This 8-bit wide multiplexed address bus (MAD0 to 7) is fed directly to the address inputs of the dynamic RAMS which form the memory planes (plane 0: U33-36, plane 1: U29-32, plane 2: U25-28). Here, the two components of the address are latched by two signals, /RAS (Row Address Select) and /CAS (Column Address Select). The signals for switching the multiplexors (ROW-

ADR-SEL) and /RAS, /CAS are derived by the timing circuitry from /ALE and the Dot Clock.

Because the multiplexed address bus is high speed and the RAM inputs are highly capacitive, the bus lines have a tendency to ring. This tendency is reduced by damping resistors R10 to R17.

After the address is transmitted, the data is put on AD0 to AD15. The direction of flow of the data (i.e., to or from the GDP) is controlled by the /DBIN output of the GDP. This signal is synchronised by the timing circuitry to produce a signal named DIRECTION which is applied to the direction control inputs of the bi-directional bus transceivers that are attached to the data lines of the RAMS (plane 0: U46, U48, plane 1: U42, U44, plane 2: U38, U40). The /OE (Output Enable) and /WE (Write Enable) signals for the RAMs are also derived using the /DBIN signal as described below.

In addition to the 16 data/address lines, the GDP outputs two address only lines, A16 and A17. These two lines are decoded to indicate which of the three memory planes is being accessed. Due to a design limitation of the GDP, these two lines must be latched before decoding. This is done by using /ALE to clock the two lines into latches U7a and b.The latched address lines are then decoded by both of the 2-to-4 line decoders in U8. Because there are only three memory planes, only three outputs of each decoder are used. Decoder U8b, which is gated by a derivative of /DBIN, provides the enable signals /WEVDBIN 0,1,2 which enable the bus transceivers for the corresponding plane. Decoder U8a is gated by a different derivative of /DBIN which is delayed by R2 and C1 to allow for the finite turn round time of the bus transceivers. The U8a outputs, which are buffered by gates U11a,b,c (and anti-ringing resistors R4, 5, 6) provide the signals /WE 0, 1, and 2. These signals pulse the WRITE ENABLE inputs of the RAMs of the corresponding plane when it is being written to.

When reading the video data for display, the desired address is placed on AD0 to AD15 as before; however, the corresponding data is not. The bus transceivers remain inactive and the addressed data is latched into parallel loading shift registers (plane 0: U45,47, plane 1: U41,43, plane 2: U37,39) by the /LOAD signal. This parallel memory data is then converted by the shift registers to serial format and clocked out on to the corresponding VIDEO 0, 1, and 2 lines by Dot Clock. The three VIDEO lines are then mixed and fed to the monitor as described above.

The process of sequentially reading out the video data to the display goes on continuously and is independent of the read/write process. Because it is a continuous process even occurring during the horizontal sync periods, it also effectively provides the necessary refresh cycles for the dynamic RAMs. The data clocked out of the RAMs during horizontal sync is ignored by the monitor because the BLANKING signal is asserted.

6G-1.6 Timing Circuitry

Only a brief description of the timing circuitry will be given here. For more details of the timing requirements, see the appropriate manuals for the GDP (Intel 82720) and the dynamic RAMs.

All the timing sequences are produced by a sequence generator formed by counter U2 (which divides the Dot Clock from the VCO) and shift register U3 which takes /ALE at its serial input and shifts it out from its Qa and Qc outputs at the Dot Clock rate, thereby producing phase shifted versions of /ALE and the phase shifted versions of /ALE are gated together. Using gates U21a,b and U22f to produce the signals /RAS and /CAS. These signals are first buffered by gates U11e,f and then fed via anti-ringing resistors R7, 8 to the RAMs. Signals /OE and DIRECTION are produced by clocking /DBIN through flip flops U10a and U9b. The output of U9b is /OE and DIRECTION is the result of gating the output of U9b with a derivative of Dot Clock through U21c. Signal /LOAD is the result of gating all the derivatives of Dot Clock together with a clocked version of /ALE through U20a. /ALE is an inverted version of the GDPs ALE output which is produced by invertor U22d.

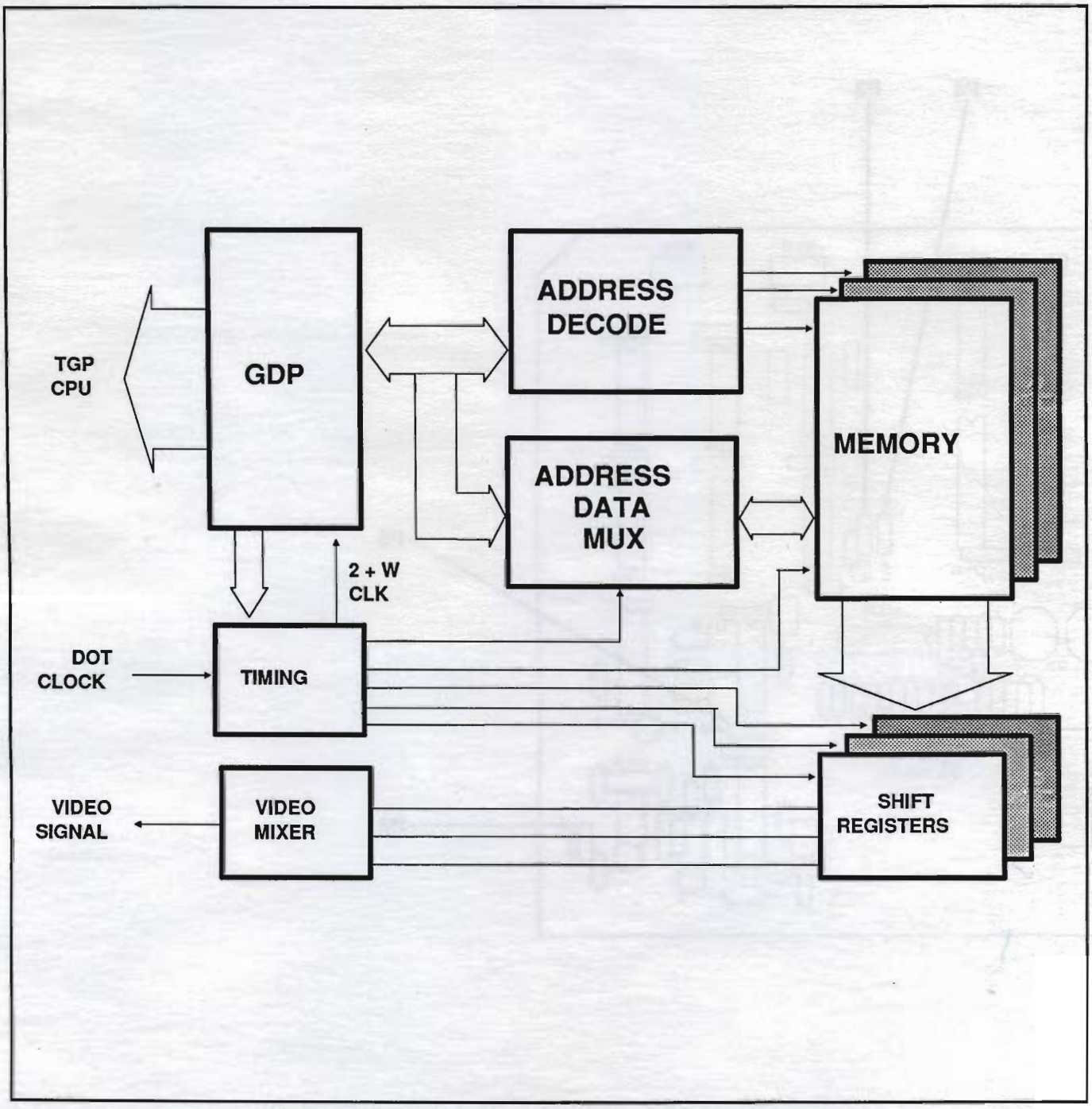

Figure 6G-1. A7 Video Display Processor PCB Block Diagram

6H-1 A8 SYSTEM GPIB PCB FUNCTIONAL DESCRIPTION

The purpose of the A8 PCB is to provide the 561 with the GPIB Talker/Listener functions necessary to interface with an external controller via the System GPIB Bus. Refer to the GPIB block diagram (Figure 6H-1), the A8 PCB parts locator diagram (Figure 6H-2), and the A8 PCB schematic (Figure 6H-3) located on the fold-out pages.

Bus controller chip U1 is a dedicated IC that handles all aspects of the operation of a GPIB interface (except that of bus controller) Devices U2, U3, U4, & U5 are GPIB bus transceivers used to communicate with the actual GPIB bus. Gates U8a and b buffer and split the bus direction control line from U1 into inverting and non inverting signals before it is applied to the transceivers U2-U5.

S1 is a 6-way switch that is used to manually set the GPIB interface address. This switch is read by the A5 Central Processor Unit PCB over the lower 6-bits of its data bus via the 6-way inverting 3-state buffer, U9. After reading the switch setting, the main processor PCB writes the selected address to a register in U1 reserved for this purpose. Gates U7b, c, d, U8c, U6a, and c perform the address decoding for U9. Gate U8d buffers and inverts the incoming system clock before it reaches U1. U8e buffers and inverts the interrupt line from U1. Gate U6d provides partial decoding of the addresses for U1.

6H-2 A10 DEDICATED GPIB PCB FUNCTIONAL DESCRIPTION

The purpose of the A10 PCB is to provide the 561 with the GPIB Talker/Listener functions necessary for interfacing with an external sweep generator via the Dedicated GPIB Bus. Refer to the A10 PCB parts locator diagram (Figure 6H-4), and the A10 PCB schematic (Figure 6H-5)

Bus controller chip U1 is a dedicated IC that handles all aspects of the operation of GPIB interface, including the handshaking protocols and timing devices. U2 and U3 are bidirectional buffers with the Dedicated GPIB Bus data and control lines.

U4 is a general purpose octal transceiver that buffers the A5 Central Processor Unit PCB data bus to and from U1. Gates U5a, b, d provide address decoding for U4. Gate U5c acts as an invertor of the CPU /RD line, which is active low (necessary because U1 requires an active high input). Resistor R2, Capacitor C11 and gates U6A/B form a Power-on Reset circuit for U1. These have input hysteresis and are used so that the relatively slowly rising voltage from the RC combination does not cause multiple spurious transitions of the gate outputs.

Device U7a is a flip-flop that functions as 1-bit write-only register. It provides a software programmable reset function. By setting this bit, the main processor PCB can initiate a hardware reset of the A10 controller U1 independantly of the power-on reset circuit. Address decoding is provided by U8. Gates U6C and d ensure that this reset register is cleared at power on.

Flip-flop U7B, together with headers P2 and P3, form a divider that divides the incoming system clock by 1 or by 2 before it is applied to U1. This was done to allow for possible future enhancements of the 561 where the system clock frequency may be increased beyond the limit that U1 can operate at.

6I-1 FRONT PANEL ASSEMBLY FUNCTIONAL DESCRIPTION

The Front Panel Assembly consists of the A11 Switch Mounting PCB and the A13 Front Panel PCB. Refer to the simplified A13 PCB block diagram (Figure 6I-1), the functional front panel block diagram (Figure 6I-2), the A11 PCB parts locator diagram (Figure 6I-3), the A11 PCB schematic (Figure 6I-4), the A13 PCB parts locator diagram (Figure 6I-5), and the A13 PCB schematic (Figure 6I-6).

6I-1.1 A11 Switch Mounting PCB

The A11 Assembly provides the interconnections for the UP, DOWN, MENU SELECT, and GRATICLE ON/OFF switches as well as the INTENSITY control for the CRT (Monitor) Assembly. This assembly is connected to the Motherboard (A9) PCB via cabling.

6I-1.2 A13 Front Panel PCB

The A13 front panel PCB, which is attached to the back of the front panel, provides the mechanical support for the instruments pushbuttons. The PCB also performs priority encoding and interrupt generation for these push buttons.

The 561 instrument bus connects between the motherboard and the A13 PCB to provide the data for the front panel LED's and for the analog spinwheel control, as well as power for the PCB. The pushbutton matrix system identifies which button on the front panel PCB has been pressed.

6I-1.3 Pushbutton Matrix

The control panel pushbuttons are wired into an x-y matrix. Since, both the X and the Y lines are numbered in the range zero to seven, there are 64 possible matrix locations. Only 39, however, are used by the front panel A13 PCB. Four locations are occupied by the A11 cursor control panel: two X lines and two Y lines go to the connector A11/P1, along with a ground line. Both the X and the Y lines are pulled to a logic HIGH (+5V) by 10K ohm resistors in two resistor packs RN1 and RN2. When a push button is pressed, that particular switches X and Y line is tied to ground. This defines each button's position in the matrix.

The eight Y matrix lines go to U9, an eight-to-three line priority encoder. When any of the eight input lines go to logic 0 (ground), U9 produces a three bit binary encoded number in the zero to seven range. This number corresponds to the selected input. If two inputs are received simultaneously, U9 selects the code from the highest priority line to be represented on the output. When a valid code is found, U9 produces a logic 0 signal on its EO output (pin 15).

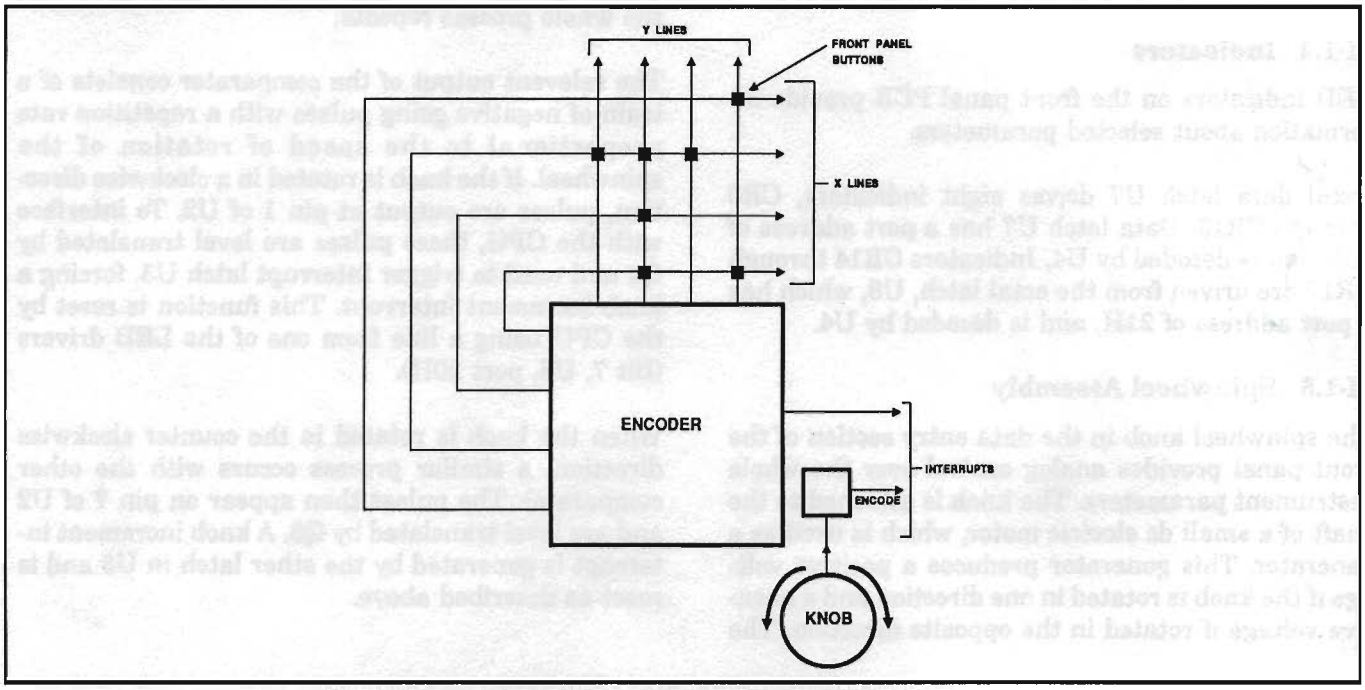

Figure 6I-1. Simplified A13 Front Panel PCB Block Diagram

The eight X matrix lines go to U10, which is also a priority encoder. U10 handles signals similarly to U9.

When a front panel pushbutton is pressed, two EO signals from U10 and U9 are ANDed together by CR4 and CR5. The resulting signal is connected to bit 4 of data port 20H (U5, a tristate buffer). The CPU then reads the signal and matrix data, allows the time that the key was pressed for to be measured, and allows suitable software debouncing action to take place.

The keyboard information therefore is read through Port 20H (U5). All port addresses are decoded by U4. From U5, bits zero to two are connected to U9 and receive the Y line information. Bits three to five are connected to U10 and receive the X line information. This provides a six bit code uniquely identifying each switch.

The ANDed EO signals from U10 and U9 are also used to trigger latch U6A, which activates the INT3 line on the bus and interrupts the central processor. This interrupt signal is cleared by any read to PORT 20H (U5). A momentary low on U6A, pin 1, will clear the latch. Since U6 is edge triggered, no further key interrupt can occur until the button is released and EO goes to logic HIGH. Data bit seven of U5 is not needed by the push button matrix system. The A11 PCB subsidiary conrol panel interfaces with the push button matrix system via connector A11P1.

6I-1.4 Indicators

LED indicators on the front panel PCB provide information about selected parameters.

Octal data latch U7 drives eight indicators, CR6 through CR13. Data latch U7 has a port address of 23H and is decoded by U4. Indicators CR14 through CR17 are driven from the octal latch, U8, which has a port address of 21H, and is decoded by U4.

6I-1.5 Spinwheel Assembly

The spinwheel knob in the data entry section of the front panel provides analog control over the whole instrument parameters. The knob is attached to the shaft of a small dc electric motor, which is used as a generator. This generator produces a positive voltage if the knob is rotated in one direction and a negative voltage if rotated in the opposite direction. The magnitude of the voltage produced is proportional to how quickly the knob is rotated.

Connector P2 provides the electrical connection between the spinwheel assembly and the front panel PCB. The signal voltage at this point contains information about the speed and direction of rotation of the spinwheel. This information is then converted to a series of pulses that interrupt the CPU via U1 and U2, together with Q1 through Q4.

Operational amplifier U1 and its associated circuitry form an integrator that can be reset by turning on Q1. When the knob is rotated, the signal at the input of U1 causes the output of the integrator to become more or less positive. This signal is dependent upon the direction of rotation and the magnitude of the signal. The magnitude of the signal is proportional to the speed of rotation of the spinwheel.

The output of U1 goes to a window comparator, U2, that has a logic HIGH trip of +8V and a logic LOW of +7V. When the spinwheel is not being rotated, the output is at +7.5V, which is at the mid-point of the window comparator.

Rotation of the spinwheel causes the U1 output to rise or fall until it lies outside the comparator window. This causes the comparator output to go to a logic LOW. Q2 then generates a pulse sufficient to turn on Q1, which discharges C1, and thus resets the integrator. If the spinwheel is still being turned, the whole process repeats.

The relevent output of the comparator consists of a train of negative going pulses with a repetition rate proportional to the speed of rotation of the spinwheel. If the knob is rotated in a clockwise direction, pulses are output at pin 1 of U2. To interface with the CPU, these pulses are level translated by Q4 and used to trigger interrupt latch U3, forcing a knob increment interrupt. This function is reset by the CPU using a line from one of the LED drivers (Bit 7, U8, port 20H).

When the knob is rotated in the counter clockwise direction, a similar process occurs with the other comparator. The pulses then appear on pin 7 of U2 and are level translated by Q3. A knob increment interrupt is generated by the other latch in U3 and is reset as described above.

6J-1 A9 MOTHERBOARD PCB FUNCTIONAL DESCRIPTION

All 561 functional PCBs are connected to the A9 Motherboard PCB. In addition, the A11 Switch Mounting PCB, the CRT (Monitor) Assembly, and the Fan Assembly are all connected to the motherboard via cables.

The motherboard routes all dc power from the A12 Power Supply PCB to all other PCBs. It provides the distribution paths for the main processor board data bus, quiet data bus and all other signal paths between PCB assemblies. The A9 PCB parts locator diagram is shown in Figure 6J-1 and the schematic is shown in Figure 6J-2.

6K-1 A12 POWER SUPPLY PCB FUNCTIONAL DESCRIPTION

The A12 PCB assembly provides seven regulated output voltages. These voltages are listed in Table 6K-1. Refer to the parts locator diagram (Figure 6K-1) and the schematic (Figure 6K-2) located on the fold-out pages.

6K-1.1 General

The ac power input to the A12 PCB assembly is provided by the line voltage selector module located on the rear panel. This module contains a line fuse and a line filter and allows the use of either of the four international line voltages: 100, 120, 220, and 240 Vac.

Two cable harnesses come from the line voltage selector module, one goes to the front panel mounted line ON/OFF switch, and the other goes to the toroidal transformer via an over temperature thermostat mounted on the power supply heat sink. The output windings from the transformer are routed though another harness to the secondary inputs on the power supply. Five connections are routed directly to P1 while the remaining two are connected to the bridge rectifier CR3. One of these wires passes through an in-line fuse and holder that protects the +5V logic supply.

The regulators are divided into two separate +5V supplies, two +15V and two –15V supplies, and a +12V supply. All output voltages are routed through P2. A multi-way connection carries these voltages through to the A9 Motherboard PCB where they are distributed around the various functions and PCBs within the instrument.

6K-1.2 Polyswitches

The polyswitches RT1, RT2 and RT3 are temperature dependent resistors used as solid state fuses. They protect the instrument from major circuit failure, that would cause a large current to flow. These devices are wired in series with the secondary windings of the 15V and 12V supplies.

Refer to the schematic (Figure 6K-2). At the onset of increased current flow the polyswitch will change its internal state and go into a high-resistance mode thus automatically limiting the current and protecting the instrument. The polyswitch is reset by switching off the line power to the instrument, removing the shorting mechanism/failure that caused it to change state, allowing the polyswitch to cool for a few minutes and then switching back on.

Table 6K-1. A12 Power Supply PCB Outputs

POWER SUPPLY	DESTINATION
+15V	A1/A2 Signal Channel Amplifier PCB A3 Signal Channel Interface PCB
–15V	A1/A2 Signal Channel Amplifier PCB A3 Signal Channel Interface PCB
+15V	A4 Sweeper Interface PCB
–15V	A5 CPU PCB A6 Text & Graphics Processor PCB A7 Video Display Processor/Monitor PCB
+12V	Fan & Monitor
+5V (2)	A1/A2 Signal Channel Amplifier PCB A3 Signal Channel Interface PCB A4 Sweeper Interface PCB A8 System GPIB PCB A10 Dedicated GPIB PCB
+5V	A5 CPU PCB A6 Text & Graphics Processor PCB

6K-1.3 Regulator Circuits

Refer to the parts locator diagram (Figure 6K-1) and to the schematic (Figure 6K-2). The linear regulators provide the supply voltages to the instruments circuits. They are arranged in three banks, each bank being supplied from a different transformer secondary winding.

All supplies use three terminal variable set regulators that feature internal short circuit protection and over temperature shut down.

VR5 is the high current three terminal regulator that is used to supply the +12V needed for the dc fan and the monitor assembly. The raw secondary ac passes onto the PCB at P1/2 and P1/3. One line passes through the polyswitch to the bridge rectifier CR2. The rectified voltage charges the reservoir capacitor C15. A safety discharge path for this circuit is provided by resistor R11.

The regulator VR5 produces the required voltage +12V, determined by the ratio of R12 and R13. Additional filtering for the set point is provided by C17.

CR13 protects the regulator from line hold up with C16 and C18 providing the input and output filtering. CR14 provides a fast discharge path for C17 if the output circuit is shorted.

VR6 and VR7 are configured in a similar way except they are used to provide the +5V lines. Two regulators are used for these supplies to distribute the power throughout the instrument to reduce local loading.

VR1 and VR3 are used to provide the two separate +15V regulators while VR2 and VR4 are used to provide the -15V supplies. VR1 and VR2 are used for the signal channel pcbs (A1, A2 and A3) and VR3 and VR4 are used to supply PCBs A4 through A7.

6K-1.4 +5V Monitor LED

The +5V supply for the digital PCBs, A5-A7 (Regulator VR6) is provided with a LED indicator monitor circuit. This circuit is comprised of LED indicator CR19 and resistor R17 across the +5V supply.

6K-1.5 Line Tick Circuit

The line tick is a logic level signal output derived from the ac supply. It is used by the main processor for timing events as well as for the A7 graphics display PCB for phase locking the screen display to the line frequency. The tick is derived from a sample of the 12V ac winding that is referenced to the the 5 volt ground at the monitor assembly. The tick output appears on P2/10 and test point TP3. It is formed from the network CR4, C26, C27, C28, R20 and R21. Q1 is used to produce the logic level with C30 acting as an output filter.

6J-1 A9 MOTHERBOARD PCB FUNCTIONAL DESCRIPTION

All 561 functional PCBs are connected to the A9 Motherboard PCB. In addition, the A11 Switch Mounting PCB, the CRT (Monitor) Assembly, and the Fan Assembly are all connected to the motherboard via cables.

The motherboard routes all dc power from the A12 Power Supply PCB to all other PCBs. It provides the distribution paths for the main processor board data bus, quiet data bus and all other signal paths between PCB assemblies. The A9 PCB parts locator diagram is shown in Figure 6J-1 and the schematic is shown in Figure 6J-2.